THE DESIGN OF HIGH FREQUENCY TRANSCONDUCTOR LADDER FILTERS

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DECLARATION OF ORIGINALITY

This thesis, composed entirely by myself, describes research performed at Wolfson Microelectronics Ltd by myself. The contributions of others to the work are acknowledged in the text where appropriate.

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The test chips were fabricated by GEC Plessey Semiconductors Ltd. Jeff Williams of Plessey Research (Caswell) assisted with data transfer and checking.

The photomicrographs of the test chips were taken by Alan Gundlach of Edinburgh University.

My parents very generously provided the PC on which this thesis has been written. MBB Deutsche Aerospace have kindly allowed me to use their printing facilities.

Most of all I wish to thank my wife, Helen, who has patiently tolerated me spending so much of the last three years working for my doctorate.

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SYMBOLS AND ABBREVIATIONS

ADC	analogue to digital converter
AGND	analogue ground (usually midrail between supplies)
ALL	amplitude lock loop
BPF	bandpass filter
bw	bandwidth
C	capacitance
C	capacitance matrix in second order equation describing passive ladder
$\mathbf{C_l}$	left hand factor of decomposed C matrix
CMFB	common mode feedback
CMOS	complementary metal oxide semiconductor, integrated circuit technology
$\mathbf{C_r}$	right hand factor of decomposed C matrix
CUT	circuit under test
Δ	difference
d.c.	direct current
F	Farad
ϕ	phase
FC	folded cascode
FCGMD	folded cascode transconductor with two conventional inputs
FET	field effect transistor
Γ	inductance matrix in second order equation describing passive ladder
G	conductance matrix in second order equation describing passive ladder
g	conductance, transconductance
GaAs	Gallium Arsenide, integrated circuit technology
gds	gate-drain conductance of a FET
gi	transconductance of transistor i
gm	transconductance
Hz	Hertz
I	current
i.f.	intermediate frequency
Ib	bias current
IMD	intermodulation distortion
Is	collector emitter junction reverse leakage current
J	input vector in second order equation describing passive ladder

k	Boltzmann's constant ($1.381\ 10^{-23}$ J/K)
K'	MOSFET gain factor
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
L	length of MOSFET channel
λ	empirical parameter in formula for MOSFET channel conductance
LC	inductor-capacitor
LD	Left Direct matrix decomposition
LI	Left Inverse matrix decomposition
LPF	lowpass filter
LTP	long tail pair
μ	micro-; frequency scaling factor
m	milli-
NSD	noise spectral density
opamp	operational amplifier
OTA	operational transconductance amplifier
p	pico-
PLL	phase lock loop
PSR	power supply rejection
Q	quality factor
q	electronic charge ($1.602\ 10^{-19}$C)
θ	impedance scaling factor
rad	radian
RC	resistor-capacitor
RD	Right Direct matrix decomposition
RI	Right Inverse matrix decomposition
RLC	resistor-inductor-capacitor
rms	root mean square
Rref	reference resistor
S	Siemens (A/V)
s	laplacian frequency variable
σ	relative amplitude scaling factor
SC	switched capacitor
sec	seconds
SG	signal generator
SPICE	Simulation Program with Integrated Circuit Emphasis
T	absolute temperature

τ	time constant
THD	total harmonic distortion
υ	matrix scaling factor
V	vector of voltages/currents in a prototype ladder
Vc	control voltage
VCF	voltage controlled filter
VCO	voltage controlled oscillator
Vds	drain-source voltage
Vgs	gate-source voltage
VLL	vector lock loop
Vout	output voltage
Vref	reference voltage
V_T	kT/q
Vt	threshold voltage of MOSFET
W	width of MOSFET channel
ω	angular frequency
X	vector of auxiliary variables in matrix decomposition

To Helen, Kathryn and Jennifer

CHAPTER 1
INTRODUCTION

1.1 Electronic filters

Frequency filters are used extensively in electronic systems, mostly in communications. A number of technologies are currently in use for the construction of filters. The technology used in a particular application is determined predominantly by the frequency of operation, though other factors such as cost, size and the nature of the response are also taken into consideration.

Filters are required at ultra high frequencies (UHF) for intermediate filtering (i.f.) in microwave links, satellite television receivers and cellular telephones. Very few types of filter can operate at such high frequency. Those used most often are surface acoustic wave (SAW) devices [1] and passive inductor-capacitor (LC) circuits. In this range LC filters take the form of strip-lines and cavity resonators [2].

At high and very high frequencies (HF and VHF) typical applications are in intermediate filtering for commercial radio and television and band limiting for sampled data video systems. In these ranges crystal and ceramic filters [3] are used as well as lumped element LC filters.

At low frequencies (<100kHz) LC filters were originally used, however the inconvenient size of inductors motivated the development of active filter circuits, incorporating valves and then transistors as the active components. The use of active resistor-capacitor (RC) filters [4] was greatly facilitated by the introduction of the monolithic operational amplifier in the late sixties. RC filters have frequently been implemented in hybrid technology, with component trimming used to obtain accurate filter responses.

Active RC filters can also be integrated on a single integrated circuit if the process concerned has suitable layers for the formation of good resistors and capacitors. However for applications requiring filters with accurate and stable transfer functions there remains the problem that the resistivity and capacitance values are highly dependent upon process parameters during fabrication and

temperature during use. For this reason a filter transfer function *shape* can be designed accurately as long as the matching between like components is good (which is usually the case) but the scaling of the transfer function in frequency will be uncertain by at best a few percent. Another problem is that in many processes only low resistivity layers (typically 20Ω per square) are available for the formation of resistors, so active RC filters in the audio range can require a very large area for the passive components.

For many applications these problems have been overcome by the development of switched capacitor (SC) techniques [5,6,7]. In an SC filter the scaling in frequency is set by capacitor ratios as a fraction of a reference clock frequency. So a transfer function can be implemented which is scaled correctly in both magnitude and frequency to the accuracy of capacitor matching (of the order of 0.1% in a good process). SC filters are always implemented in a field effect transistor (FET) technology due to the requirement for very high input impedance in the amplifiers used.

SC filters have been applied successfully to many applications and are used routinely in analogue CMOS circuits. There are however a number of application areas, such as video signal processing, in which they are not easily applicable due to the high signal frequencies involved. Usually the clock frequency is designed to be several tens of times the passband frequencies, and the fastest rate at which CMOS SC circuit can settle satisfactorily is a few MHz, therefore such filters are not often designed with passband frequencies greater than several tens of kHz. Occasionally SC filters have been reported with passband frequencies greater than 1MHz [8,9], however they are difficult to design, consume a large amount of current and generate a lot of clock noise. The requirement for fast settling amplifiers (still with high input impedance) can be met by using GaAs technology [10,11], but this solution is expensive both in terms of the cost of the process and the power supply current used.

Another drawback of SC filters in high frequency applications is the fact that they are "sampled data" in nature. Some applications, such as anti-alias filtering for video ADCs, require a continuous time solution.

Both of the reasons described above have motivated the search for a type of monolithically integrated filter which is accurately tunable, continuous time, and which can operate at high frequencies. This thesis is a study of a very promising candidate: the transconductor ladder filter.

The transconductor [12;13,14] is an active circuit which generates an output current directly proportional to an input voltage, the constant of proportionality (transconductance) being adjustable by a d.c. bias (or control) voltage. Its function

can be analogous to that of both the resistors and opamps in an active RC filter, therefore the only other components that are essential to complete a transconductor filter are capacitors. However, additional components are usually required to form a "control loop" which sets the control voltage such that the filter is correctly scaled in frequency with respect to the frequency of a reference clock signal.

Like other active filters, a transconductor filter can be designed as a cascade of biquadratic stages [6,16,17,18], or as a simulation of a passive RLC ladder [19,20,64]. The former architecture appears to be preferable for those transconductor filters which are of such high frequency and selectivity that multiple control loops are required [16,18]. This thesis is concerned with the remainder of applications, in which ladder filters are generally preferable due to their lower sensitivity to component value tolerances [21].

Transconductor filters have been studied for many years, but it is clear from the literature that they are still predominantly the subject of academic research, very few having been used in commercial applications. This state of affairs is understandable since the design of the filters, the control circuitry and the transconductors themselves presents very challenging problems. It is hoped that the work described in this thesis has overcome some of these problems and will bring forward the day when transconductor filters are used successfully in commercial applications.

1.2 The transconductor and other amplifiers

The transfer function of an ideal transconductor can be written:

$$I = g(V_C)V_{in} \qquad (1.2\text{-}1)$$

where I is the output current, V_{in} is the input voltage, V_C is the control voltage and g (the transconductance) is a monotonic frequency-independent function of V_C. The transconductor symbol is shown in figure 1.2-1. Although shown here, the connection of V_C is often omitted in this thesis since it can be treated as a globally routed signal, like other bias and supply voltages needed by the transconductor. We adopt the convention that a positive output current is conventional current flowing out of the transconductor. It should be noted that this differs from the definition of the voltage controlled current source (VCCS) in the simulation program SPICE [22]; the VCCS being a useful macromodel for a transconductor.

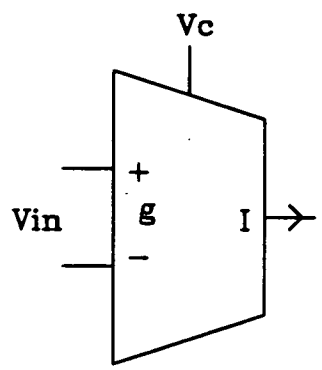


Figure 1.2-1

Symbol for a transconductor with differential input and single ended output

In general it is desirable to design transconductor filters to be fully differential. The reasons for this will be discussed in the following chapter. The symbol for a fully differential transconductor is shown in figure 1.2-2. Its transfer function is

$$I+ = -(I-) = g(V_C)V_{in}. \qquad (1.2\text{-}2)$$

The ideal transconductor has infinite output impedance. A departure from this condition results in not all of the output current being delivered to the desired load, which can have serious consequences for the performance of the filter in which the transconductor is used.

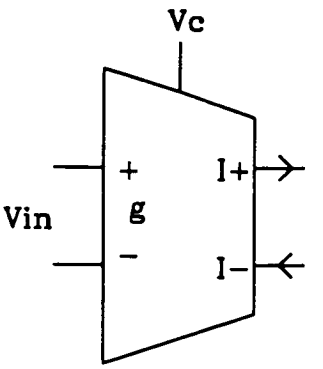


Figure 1.2-2 Symbol for a fully differential transconductor

The transconductor is very similar to the operational transconductance amplifiers (OTA's) used regularly in switched capacitor circuits [23]. The difference is that the voltage to current conversion of the OTA is not required be linear, since it is the d.c. voltage gain in the settled state that is of primary importance in an SC circuit. Terms used in the literature are not always consistent with those defined here. OTA's are often referred to loosely as opamps, and transconductors as OTA's. Table 1.2-1 summarizes the principal characteristics of the ideal transconductor, OTA and opamp.

Circuit	Input	Output	Transfer function	Input Z	Output Z
transconductor	voltage	current	linear variable transconductance	infinite	infinite
OTA	voltage	current	infinite transconductance	infinite	infinite
operational amplifier	voltage	voltage	infinite voltage gain	infinite	zero

Table 1.2-1 Comparison of different ideal amplifiers

The effects on filter performance of some departures from the ideal transconductor behaviour [24] are described and illustrated in appendix A.

In a transconductor filter, summation can be performed easily by connecting transconductor outputs together, as shown in figure 1.2-3. However in such an arrangement there may be unnecessary duplication of some components internal to the transconductor, such as those used in output and common mode feedback stages. In that case it is more economical to design a multiple input transconductor, the

symbol for which is shown in figure 1.2-4. Such a circuit has as many sets of V to I converting components as required, whose outputs are summed prior to the final stages of the transconductor.

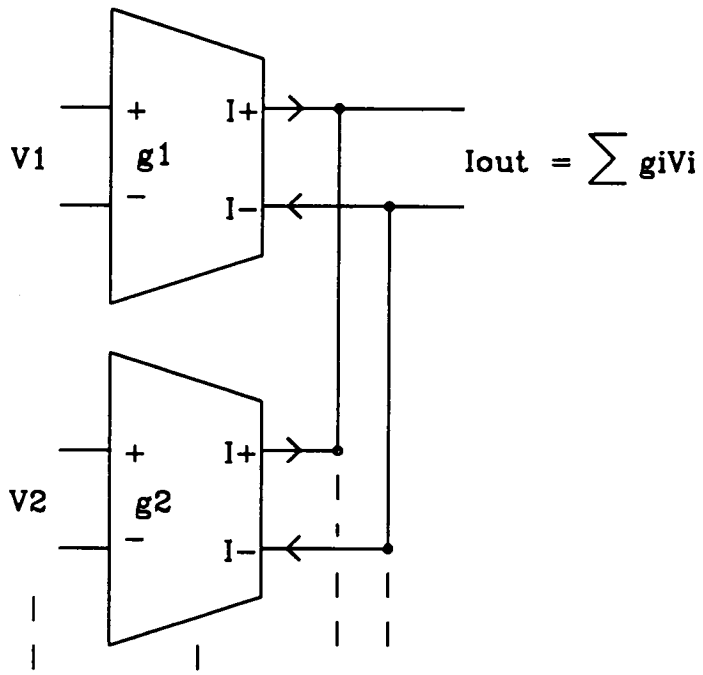


Figure 1.2-3 Summation by connecting transconductor outputs together

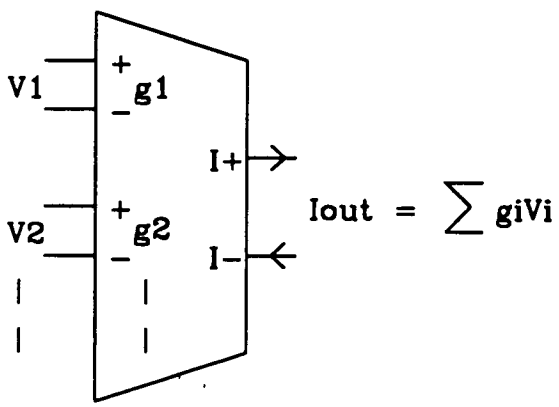


Figure 1.2-4 Summation using a multiple input transconductor

As is the case for all active filters, the basic building block used to construct a transconductor filter is the integrator. A transconductor integrator can be formed simply by connecting a capacitive load to the output of the transconductor, as shown in figure 1.2-5. In a practical fully differential circuit, the load would consist of at least two capacitors; this is discussed in detail in chapter 3.

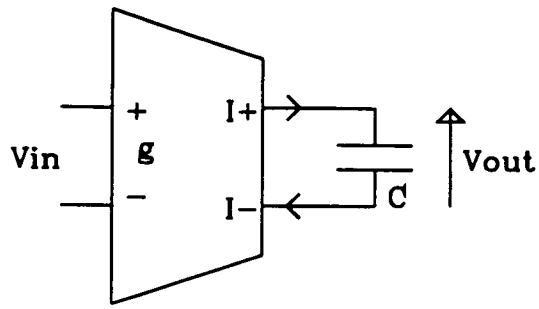


Figure 1.2-5 Open loop transconductor integrator

The transfer function for this configuration is

$$V_{out} = \frac{g(V_C)}{sC} V_{in}. \qquad (1.2\text{-}3)$$

We refer to this as an "open loop" integrator because the load capacitor is not connected as the feedback component of an amplifier. The advantage of the open loop integrator is its simplicity. The disadvantages are that *i.* the parasitic capacitance at the output of the transconductor appears in parallel with the designed load and hence tends to cause a first order error, *ii.* the transconductor output impedance is required to be very high (typically at least 10^3 times the transconductance) and *iii.* this integrator has no low impedance nodes so a filter constructed from it cannot have unidirectional capacitive signal paths (the utility of which is demonstrated in chapters 6 and 7).

In contrast, the "closed loop" transconductor is shown in figure 1.2-6. In this case an opamp is included (or an OTA if there is no resistive load), around which load capacitors are connected as feedback. This is equivalent to an active RC integrator with the resistor replaced by a transconductor. The closed loop integrator solves the three problems of the open loop integrator described above because (respectively): *i.* there is no transconductor parasitic capacitance appearing in parallel with the designed load, so such parasitics can only cause second order errors, *ii.* the transconductor drives into a virtual earth and hence does not have to have such a high output impedance, and *iii.* the closed loop integrator has low impedance outputs and inputs (the virtual earth is the low impedance input). The main trade-off for these benefits is that significantly more current and chip area are required per integrator to provide the extra amplifier, even though the design of the transconductor itself is simplified (due to the relaxed output impedance requirement). Moreover, the

bandwidth of the amplifier has to be much greater than that of the integrator, which is a problem since we have identified high frequency filters to be of primary interest.

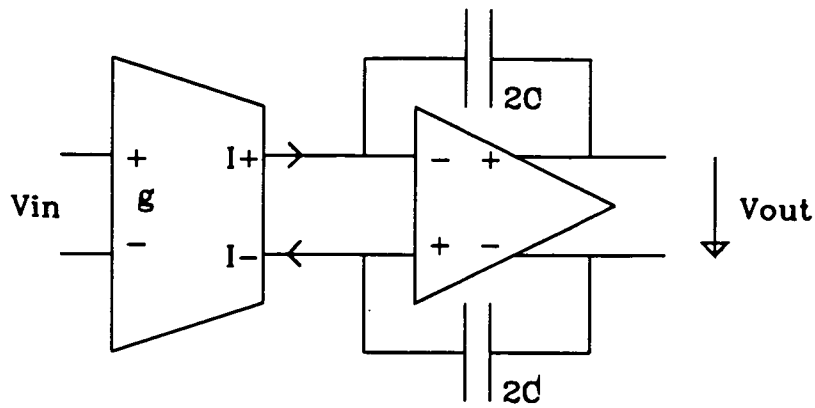


Figure 1.2-6 Closed loop transconductor integrator

In this thesis we shall consider the design of filters principally using open loop integrators, which is the more challenging problem both from the point of view of the transistor level design of the transconductor and the derivation of the filter structure. The techniques developed can also be applied where appropriate to the design of filters using closed loop integrators.

1.3 Overview of this thesis

The subject of transconductor filter design can be divided into three parts: transconductors, filter structures and control circuitry. The first of these is reviewed in chapter 2 and the other two in chapter 3. It is noticeable that the literature is particularly well endowed (in quantity) with suggestions for transistor level implementations of the transconductor. This is understandable because there is not one method of achieving linear voltage to current conversion with transistors that stands clearly above the others. It is rather the case that,of the good transconductor circuits that have been proposed, each may be the best choice in a particular area of application. The parameters that affect this choice include: power supply voltage, current available, frequency of operation, linearity required and maximum signal size.

In chapter 4 an original CMOS transconductance cell is described which is best suited to applications requiring high frequency of operation and high linearity within a low power supply. In chapter 5 the advantages of designing transconductors with folded cascode output stages are demonstrated. Also, two enhancements to the standard folded cascode structure are proposed. The first is the addition of low impedance inputs (in addition to the normal inputs). These allow the use of unidirectional capacitive branches in filters based on open loop integrators, and thereby increase greatly the number of ladder filter structures that can be designed. The second enhancement provides control of the phase response of the transconductor by means of a variable d.c. voltage. This may be used to compensate actively for the effects of parasitic poles. Examples of folded cascode transconductors are given which are based on the transconductance cell introduced in chapter 4.

In chapter 6 a set of algebraic methods for the design of transconductor ladder filters is presented. These represent a structured method which may be used as the basis for computer aided design tools [65]. More importantly they provide an abstract representation of the ladder which can be used to find superior active filter circuit that are far from intuitively obvious. In particular, new circuits for bandpass ladders are derived which could not be obtained using conventional signal flow graph methods.

Using the methods described in this thesis, a number of transconductor ladder filters have been designed for a 1μ CMOS process. These have been fabricated on two test chips, along with a frequency control phase lock loop and high frequency buffer amplifiers to drive the filter outputs off chip. In chapter 7 the design and evaluation of these circuits and the necessary test equipment are described.

Chapter 8 presents the conclusions of this work and makes suggestions for future research.

CHAPTER 2
REVIEW OF TRANSCONDUCTOR DESIGN

2.1 Introduction

This chapter presents a survey of circuits that other investigators have proposed to approximate to the ideal transconductor defined in section 1.2. Original transconductor circuits developed by the author are analysed in chapters 4 and 5.

The fact that so many circuits have been tried reflects the difficulty of the design task and contrasts sharply with the state of affairs in switched capacitor circuit design where a particular type of amplifier (the folded cascode [23]) was accepted rapidly as a standard for most applications. Transconductors are harder to design because of their requirement for linearity as well as high gain; in RC and SC circuits the amplifiers need have only high gain, the linearity being provided by passive feedback components.

The circuits are categorised by technology. Three sections are devoted to CMOS circuits, since that has been by far the most popular technology for transconductors as well as modern analogue signal processing circuits in general. For each circuit, the method used to obtain a linear voltage to current transfer function is discussed. Analytical expressions are derived using the device equations given in appendix B. In the interest of brevity, other important design issues such as noise, high frequency performance, current consumption, and gain are given a more qualitative treatment.

This survey is not intended to be an exhaustive list of transconductors. The objective of the chapter is rather to explain the main ideas that engineers have drawn upon when designing such circuits.

2.2 The CMOS long tail pair and its derivatives

The long tail pair (LTP) is a ubiquitous configuration in analogue IC design [25,56] providing the differential input stage for the majority of amplifier designs. In bipolar circuits a more sophisticated input is sometimes required to minimise input bias current, but in FET amplifiers the extremely high gate impedance allows the simple LTP input to be used in virtually all cases, the only common exception being when a single-stage class AB amplifier is required [26].

The CMOS LTP is attractive as a transconductor for a number of reasons. Firstly, being single-stage it is compact and has good high frequency performance. Its parasitic poles are associated with transmission line effects in the input devices and are at higher frequencies than would be the non-dominant poles of a multi-stage amplifier [27]. There is also a transmission zero due to the gate-drain overlap capacitances of the input transistors. Secondly, it can be used fully differentially to maximise power supply rejection (PSR), dynamic range and the cancellation of second order harmonic distortion.

A fully differential CMOS LTP transconductor with n-type inputs is shown in figure 2.2-1. In fact p-type input stages are often preferable because they have larger transistors for a given transconductance and therefore match better. N-type inputs are generally shown in this chapter for clarity.

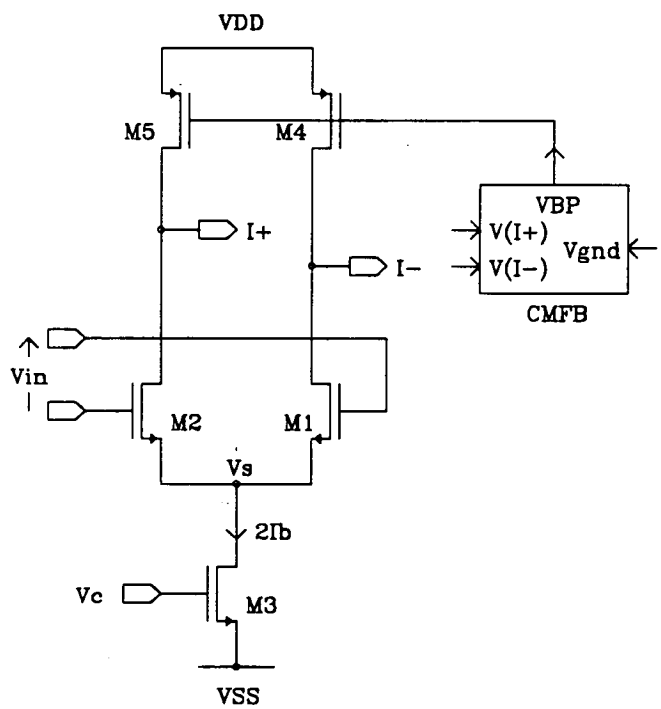


Figure 2.2-1 Fully differential long tail pair transconductor

A differential input voltage V_{in} is applied between the gates of matched transistors M_1 and M_2 and the output current is taken as the difference between their drain currents. M_3 acts as the long tail current sink; the current in this device, $2I_b$, determines the value of the transconductance and is set by the control voltage V_c. M_4 and M_5 are identical active loads biassed by V_{BP}. V_{BP} is generated by the common mode feedback (CMFB) circuit such that the mean (common mode) of the two output voltages of the transconductor remains close to a set bias level, usually a signal ground midway between the two supply voltages. A suitable CMFB circuit is given in figure 2.2-2.

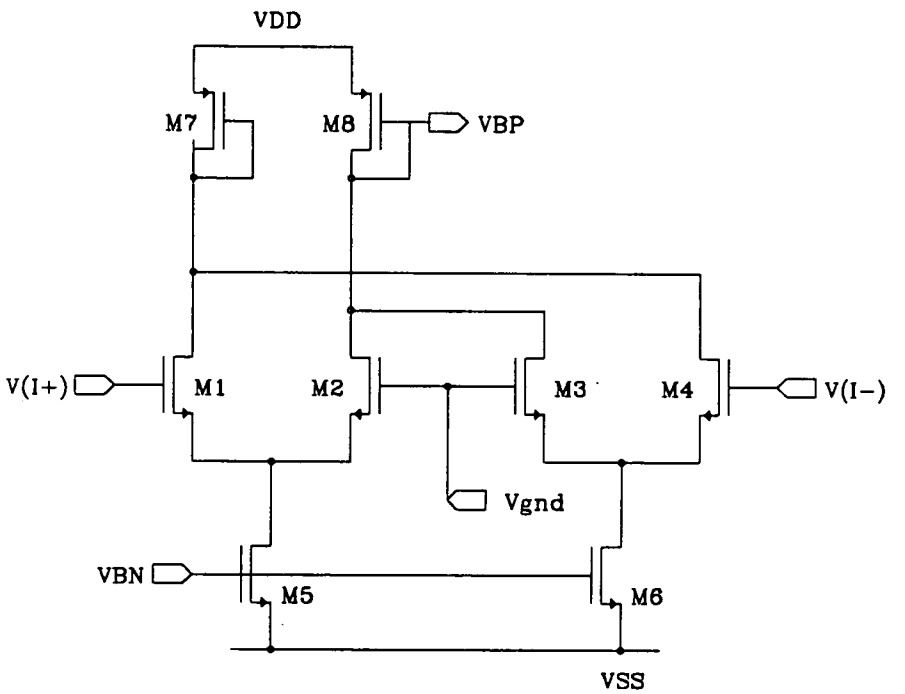


Figure 2.2-2

Common mode feedback circuit for use with fully differential transconductors

A simple transfer function can be derived for the LTP by neglecting channel length modulation and the body effect. Applying (B-3) we write the channel currents of M_1 and M_2 as:

$$I_1 = 0.5\beta[V_{in}/2+V_{gnd}-V_s-V_t]^2 \qquad (2.2\text{-}1)$$

$$I_2 = 0.5\beta[-V_{in}/2+V_{gnd}-V_s-V_t]^2, \qquad (2.2\text{-}2)$$

where V_s is the common source voltage, and the signal ground V_{gnd} is the quiescent gate voltage of M_1 and M_2. The output current is found by eliminating (V_{gnd}-V_s-

V_t) from (2.2-1) and (2.2-2) and then solving for $(I_1-I_2)/2$, making use of the fact that $I_1+I_2=2I_b$:

$$I = \sqrt{\frac{\beta I_b}{2}} V_{in} \sqrt{1-\frac{\beta V_{in}^2}{8I_b}} \tag{2.2-3}$$

$$= gm V_{in} \sqrt{1-\frac{V_{in}^2}{(2V_x)^2}}. \tag{2.2-4}$$

V_x is the quiescent value of the excess voltage $(V_{gs}-V_t)$ for each input device. The transconductance of the fully differential LTP, $gm=\sqrt{\beta I_b/2}$, equals half the tranconductance of each of the input. It should be noticed that in a conventional single ended LTP the active load devices are connected as a current mirror and the output current is (I_1-I_2), twice the value for the fully differential circuit. In fact it is generally true that a transconductor with single-ended output has twice the transconductance as the fully differential circuit formed from the same differential input stage.

Equation (2.2-4) can be expanded using the binomial theorem:

$$I = gm V_{in} - \frac{\beta^{3/2}}{8\sqrt{2I_b}} V_{in}^3 + \ldots \tag{2.2-5}$$

The expansion (2.2-4) contains only terms of odd order, due to the symmetry of the circuit. It is clear from (2.2-4) that good linearity is dependent upon a large value of V_x. Unfortunately the values to which V_x is limited by the headroom available are generally insufficient, particularly for a 5V process and when tolerance is allowed for temperature and process variations. For example, (2.2-4) predicts that for V_x = 1V the error in current will be 1% for V_{in} = 300mV, which will be unsatisfactory for most applications. The circuits described later in this section all attempt to improve upon the linearity of the LTP whilst preserving its more beneficial features. The methods that have been used to obtain greater linearity include: cross-coupling, degeneration, and adding a V_{in}-dependent current to $2I_b$.

To obtain an expression for the output impedance of the LTP, we make the assumption that for small differential signals the voltage V_s has a negligible a.c. component. Then the impedance of each output node is equal to the parallel combination of the drain-source impedances (r_{ds}) of the input and load devices connected to that node, i.e. we can write:

$$R_{out} = r_{ds1} \| r_{ds4} \tag{2.2-6}$$

It is necessary to draw the length of the input devices as small as possible in order to maximise the frequencies of the parasitic poles associated with them, whereas the active load devices can be made relatively long. Therefore the channel length modulation factor λ will be correspondingly larger for the input devices and the output impedance of the transconductor will be dominated by it. Using equation (B-6) we can then write:

$$R_{out} = 1/\lambda I_b. \tag{2.2-7}$$

The gain of the LTP is given by

$$A = gm(0)R_{out} \cong \sqrt{\frac{2\beta}{\lambda^2 I_b}} \tag{2.2-8}$$

where β and λ refer to M_1. Using the approximate relation (B-8) for λ this can be written

$$A \cong \sqrt{\frac{2WLK'}{\theta^2 I_b}} \tag{2.2-9}$$

Evaluating (2.2-9) with typical parameter values indicates a gain in the region of 35dB. Such gain is just about feasible for a lowpass filter of reasonably low order, but not for a bandpass filter where it can cause serious distortion of the passband shape. This conclusion applies not just to the LTP but to any simple single stage transconductor. For bandpass filters it is preferable to obtain high output impedance and gain by the use of cascode devices, which are discussed in chapter 5. However it is worth mentioning an alternative solution proposed by Khorramabadi and Gray [24,27]. They obtained an analytical expression for the excess phase caused by transmission line effects in the input transistors and designed the length of these devices such that it was cancelled by the phase lag associated by the finite gain at the centre frequency of the bandpass filter. Since the cancellation is frequency dependent it can only be used for narrow band filters. Unfortunately the process parameters upon which this technique relies are not usually well enough characterised for it to be useful. In any case it is undesirable for the design of what should be a 'black box'

component to be influenced in such a detailed way by the particular filter response being implemented.

Greater linearity can be obtained by cross-coupling two LTPs with opposing polarity [27] as shown in figure 2.2-3.

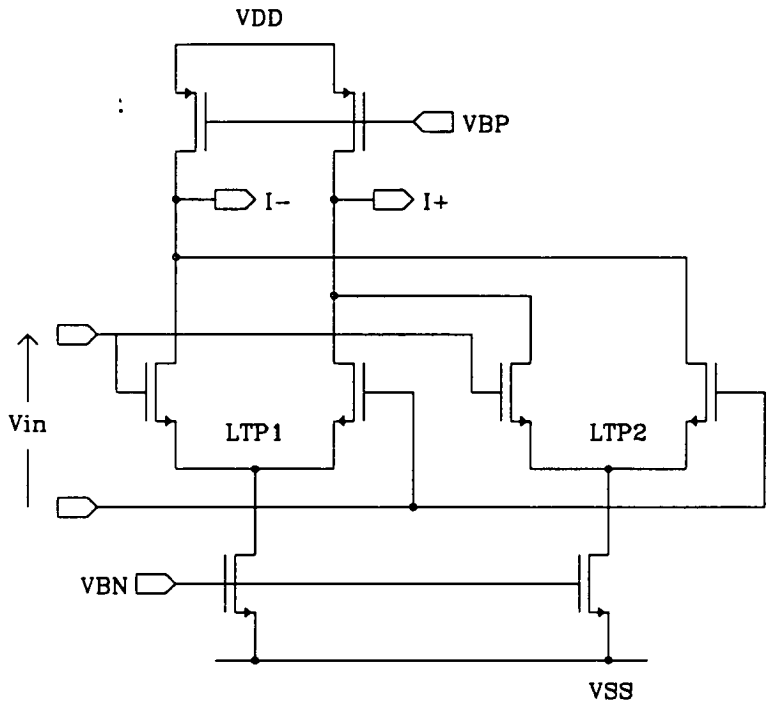


Figure 2.2-3 Cross-coupled long tail pairs

The two LTPs share a single set of active load and CMFB transistors similar to those in figures 2.2-1 and 2.2-2. The device sizes and bias currents are ratioed such that the dominant third order non-linearity term is cancelled. To obtain the transfer function for this configuration (2.2-4) is written for each of the LTPs and the difference between the two equations is taken, giving:

$$I = (gm_1 - gm_2)V_{in} - \left[\frac{\beta_1^{3/2}}{8\sqrt{2Ib_1}} - \frac{\beta_2^{3/2}}{8\sqrt{2Ib_2}}\right]V_{in}^3 + \ldots \qquad (2.2\text{-}10)$$

The small signal transconductance is obviously given by:

$$gm = gm_1 - gm_2. \qquad (2.2\text{-}11)$$

Assuming that the process parameter K' is identical for the input devices of both LTPs, the condition implied by (2.10) for its third order term to vanish is:

$$\left[\frac{(W/L)_1}{(W/L)_2}\right]^3 = \left[\frac{I_{b1}}{I_{b2}}\right]. \qquad (2.2\text{-}12)$$

Since there are four independent design variables and only two equations to be satisfied, the choice of devices sizes and bias currents can involve other considerations, such as the power consumption. An efficient way to satisfy (2.2-11) and (2.2-12) is to make gm_1 just greater than gm so that $gm_2 << gm$. In this case I_{b1} is only slightly greater than the I_b of a simple LTP and I_{b2} is small compared to both. A small value of I_{b2} makes the third order non-linearity of the second LTP relatively large, so at this order there is *not* a compromise between linearity and power consumption. A lower limit on the value of I_{b2} will be placed by considerations such as the accuracy of the current source and the fifth order harmonic distortion term.

Since the cross-coupled LTPs are both connected to V_{in}, the input capacitance will be somewhat higher than that of the simple LTP. The thermal noise will also be greater, particularly if the value of gm_2 is designed to be low, however the overall SNR will generally be much greater than that of the simple LTP due to the reduction in harmonic distortion. The output impedance and high frequency performance of the cross-coupled LTP is similar to that of the simple LTP. However it is interesting to note that the frequency of the transmission zero associated with the gate-drain overlap capacitance of the input devices is increased due to the opposing polarity of the two pairs. This cancellation can be made complete in principle by drawing equal widths for all four input transistors, but it may be preferable to design for equal lengths for best matching between the transistors.

The second method we consider for linearising the LTP is source degeneration, analogous to emitter degeneration in bipolar circuits. In practice the degeneration is usually performed by active components simulating a voltage controlled resistance but first we illustrate the principle of degeneration with reference to ideal resistors. Figures 2.2-4 and 2.2-5 show two ways in which the LTP can be source degenerated; in fact these circuits have the same transfer function.

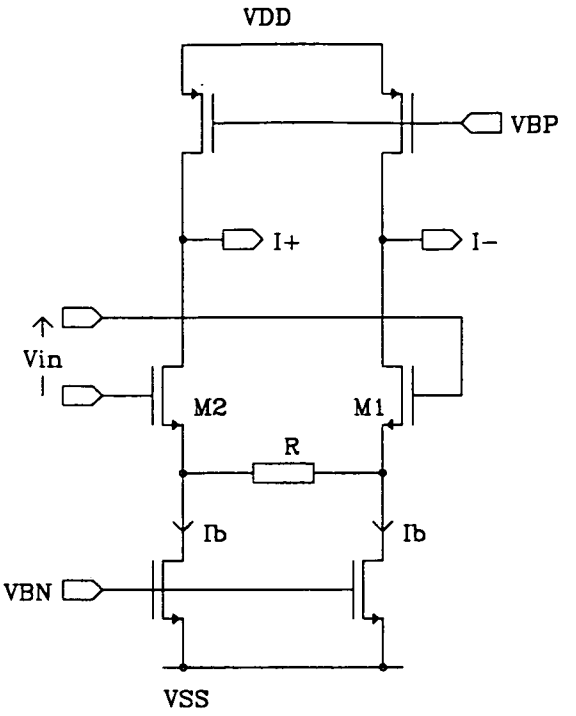


Figure 2.2-4 LTP degenerated with a single resistor and two tail current sources

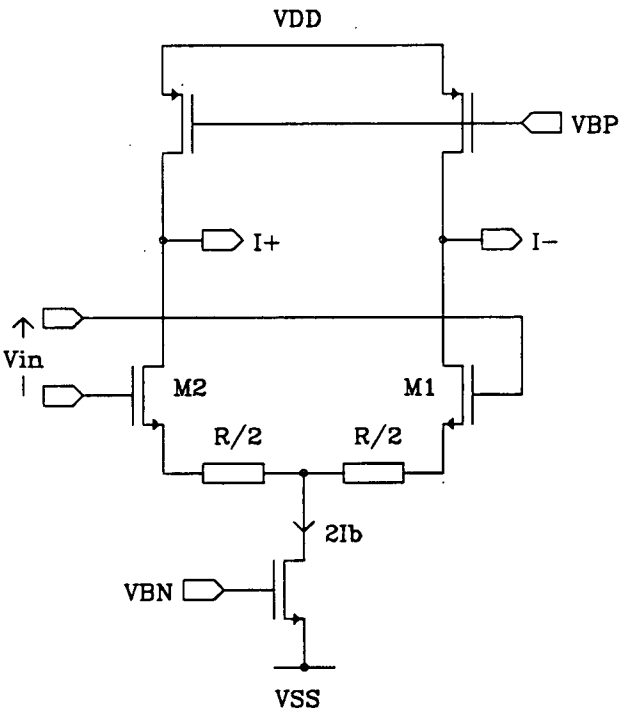


Figure 2.2-5 LTP degenerated with two resistors and a single current source

For the simple LTP the input voltage is divided entirely between V_{gs1} and V_{gs2}, but

for the degenerated circuits:

$$V_{in} = V_{gs1} - V_{gs2} + IR \tag{2.2-13}$$

where as before the output current $I = (I_1 - I_2)/2$. Therefore the new transfer function can be obtained by substituting $(V_{in}-IR)$ for V_{in} in equation (2.2-3). This gives:

$$I = gm(V_{in}-IR)\sqrt{1-\frac{(V_{in}-IR)^2}{V_x^2}}, \tag{2.2-14}$$

which can be rearranged:

$$I = gmV_{in}\left[\frac{T_{nl}}{1+gmRT_{nl}}\right] \tag{2.2-15}$$

where the non-linearity term

$$T_{nl} = \sqrt{1-\frac{(V_{in}-IR)^2}{V_x^2}}. \tag{2.2-16}$$

As R tends to zero (2.2-15) reduces to the non-degenerated transfer function (2.2-4). In the opposite limit, defined by $R >> 1/gm$, (2.2-15) reduces to:

$$I = V_{in}/R. \tag{2.2-17}$$

This expression is understood qualitatively as follows. A degenerating resistor of large value draws little current compared to the quiescent current in each input device, therefore the V_{gs} of the input devices is modulated insignificantly by the input signal. In this case all of the differential input signal is transferred to the resistor with a common-mode level shift of V_{gs}. In contrast with the case of cross-coupled LTPs, improved linearity is obtained at the expense of increased power consumption.

For a practical transconductor circuit a voltage controlled resistance is required so that the transconductance will be tunable. This is provided most simply by the channel conductance of a MOSFET operating in triode mode, controlled by its gate voltage [28]. A transconductor employing this form of degeneration is shown in figure 2.2-6.

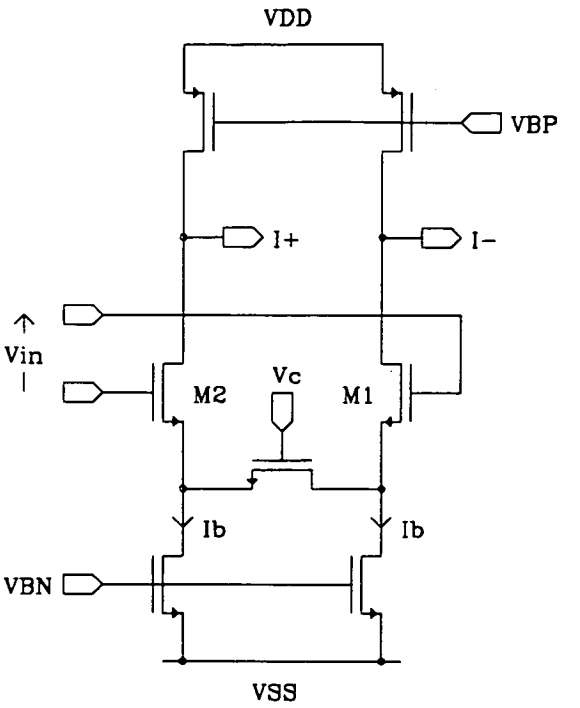


Figure 2.2-6 Long tail pair degenerated with a MOSFET biassed in triode mode

The linearity of this configuration is dependent upon the signal being applied fully differentially with no common mode signal component, i.e. the excursions of the drain and source voltages from their quiescent value should always be equal and opposite. If we make the assumption that the transconductance of the input devices is much greater than the channel conductance of the degenerating transistor, then these voltages are respectively $V_{in}/2$ and $-V_{in}/2$. The gate voltage is the d.c. control voltage V_c (defined here with respect to the quiescent drain/source voltage of the degenerating transistor). To find an expression for the transfer function we use equation (B-9) for the channel current in the triode device. Writing the terminal voltages explicitly this equation can be reexpressed:

$$I_{ds} = \beta\left[V_g - V_t - V_s - \left[\frac{1+\delta}{2}\right](V_d - V_s)\right](V_d - V_s). \qquad (2.2\text{-}17)$$

Subsituting $V_g=V_c$, $V_d=V_{in}/2$ and $V_s=-V_{in}/2$ into (2.2-17) gives the output current of the transconductor:

$$I = \beta(V_c - V_t - \delta V_{in})V_{in} \qquad (2.2\text{-}18)$$

In elementary treatments of the MOS transistor the parameter δ is given the value zero. If this were the real value then the transconductance predicted by (2.2-18)

would be completely linear. Unfortunately in practice δ departs significantly from zero causing a large second order harmonic distortion [29]. The fact that the dominant distortion term is of even order indicates that the circuit is essentially asymmetric for non-zero values of V_{in}. This is a surprising conclusion since figure 2.2-6 is visually symmetrical. It is explained by the fact that the conductance of the triode transistor is always lower at the end of higher potential. The circuit is only symmetrical for $V_{in} = 0$ when the conductance of the channel is uniform.

It is clear from (2.2-18) that V_c should be made as large as possible, firstly to reduce the relative magnitude of the distortion term and secondly to minimise the mismatch error caused by variations in V_t between transconductors. However both of these error sources can be greatly reduced in significance by cross-coupling two triode-degenerated LTPs [28] as shown in figure 2.2-7.

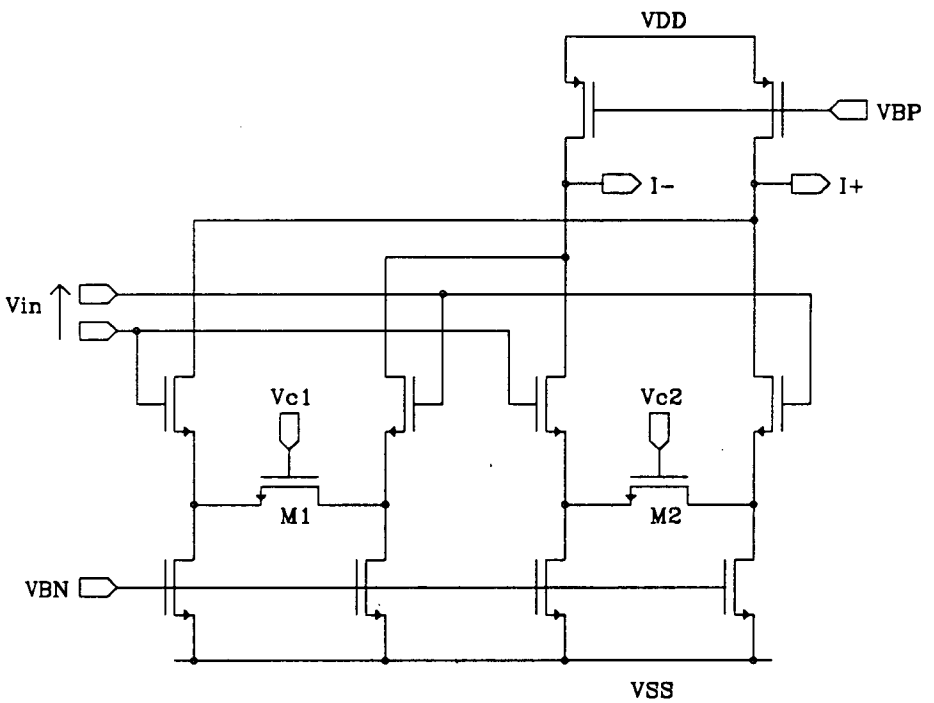


Figure 2.2-7 Cross-coupled triode-degenerated long tail pairs

The two pairs are identical except that they take different values of control voltage, V_{c1} and V_{c2}. If the two devices have equal values of β, δ and V_t, then (2.2-18) predicts that the transfer function of the cross-coupled circuit will be:

$$I = \beta(V_{c1}-V_{c2})V_{in}. \qquad (2.2\text{-}19)$$

Cross-coupling cancels the asymmetry of the each degenerated pair, as a result of

which the sensitivity of the transconductance to common mode noise in V_t, the substrate or the signal itself is removed. Of course this cancellation is only as accurate as the matching of the two degenerated pairs. Other sources of distortion are mobility variation and body effect in the triode transistors (since they obviously cannot be bulk-source connected) and modulation of V_{gs} in the input devices. The price paid for the improved linearity of the cross-coupled circuit is a further increase in power consumption and thermal noise.

A second form of source degeneration [30,31] is applied in the circuit shown in figure 2.2-8. We refer to this as "adaptive degeneration" since the conductance of the degenerating devices M3 and M4 is deliberately modulated by the input voltage. This is not to be confused with another linearising technique called "adaptive biassing", which will be described later in this section.

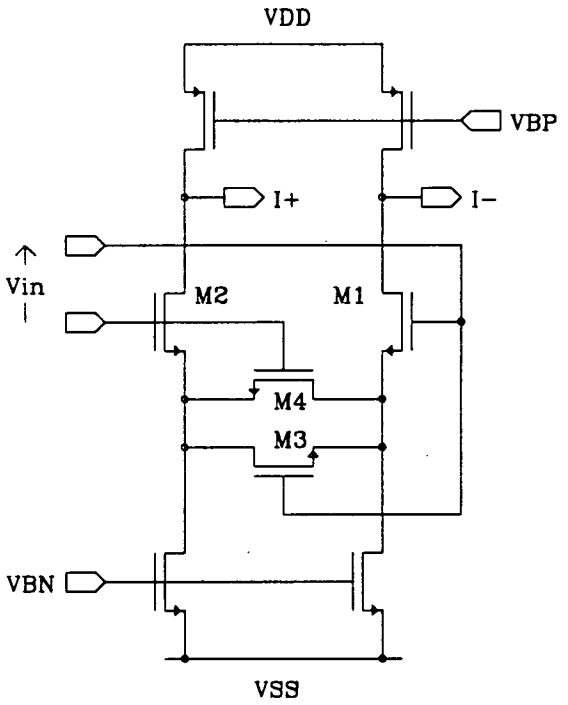


Figure 2.2-8 Adaptively degenerated long tail pair

For small values of input voltage M_3 and M_4 are both in triode mode and degeneration is provided by their drain-source conductances, with the corresponding *negative* second order distortion term. However when V_{in} becomes sufficiently large, one of M_3 and M_4 (depending upon the polarity of the input signal) goes into saturation mode. The degeneration is then dominated by the *trans*conductance of this device which has a *positive* second order term. The value of V_{in} at which the polarity of the second order term changes is determined by the ratio of the β of M_1 and M_2 to

that of M_3 and M_4, which is equal to the ratio of aspect ratios if a constant value of K' is assumed. This ratio can therefore be designed for maximum linearity. The optimum value usually lies between 6 and 7. The nominal value of transconductance is lower than that of a simple LTP with the same value of bias current and input device size by a factor approximately equal to $(1+\beta_1/\beta_3)$. The transconductance is controlled by the bias current.

The adaptively degenerated LTP has the same sensitivity to common-mode noise as the triode-degenerated LTP due to the presence of second order terms even in the ideal transfer function. However it allows a given degree of linearity to be obtained with less current than required for the cross-coupled triode degenerated LTP.

A third degeneration method takes advantage of the fact that a fully differential transconductor with its outputs connected to its inputs of opposing polarity acts as a floating resistor [32]. Figure 2.2-9 shows an LTP degenerated by such a transconductor.

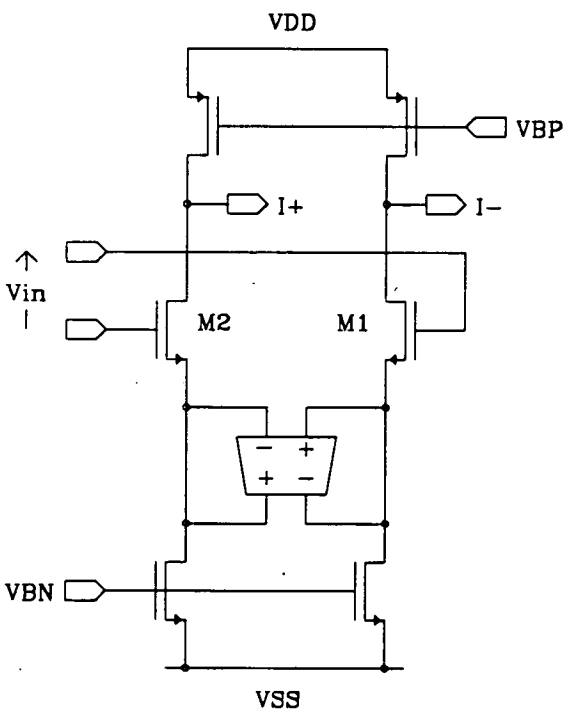


Figure 2.2-9 LTP degenerated by a transconductor configured as a floating resistor

The degenerating transconductor can itself be a simple LTP, in which case figure 2.2-9 becomes equivalent to the transistor level circuit shown in figure 2.2-10.

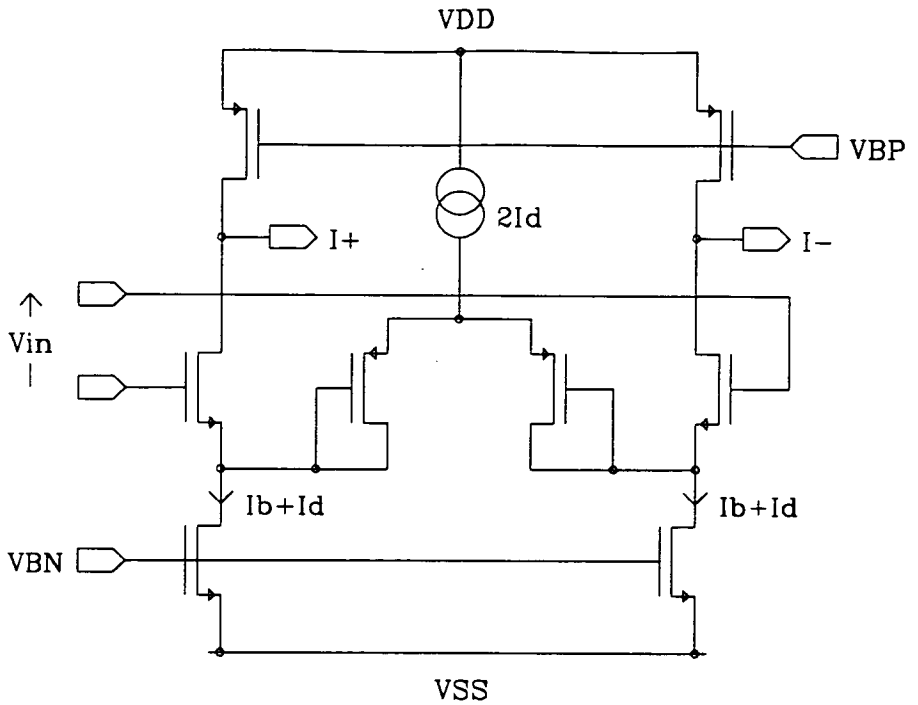


Figure 2.2-10 One LTP degenerated by another LTP configured as a floating resistor

In principle more than two LTPs can be connected together in this way. For a connection of N LTPs the input voltage is effectively divided by N, so the transfer function of such a circuit will be similar to (2.2-4) with V_{in}/N substituted for V_{in}. For a given value of transconductance the relative magnitude of the third harmonic is then reduced by the factor N^2 at the expense of N times the current consumption of the simple LTP. Even discounting the high current consumption these circuits are not attractive, because their complexity leads to poor high frequency performance.

Another method that has been tried to linearise the LTP is the addition of a term proportional to V_{in}^2 to the long tail current; we refer to this here as "adaptive biassing" [33,34]. To illustrate the principle we rewrite the transfer function (2.2-4) of the LTP in a slightly different form:

$$I = V_{in}\sqrt{\beta(2I_b-\beta V_{in}^2/4)}. \qquad (2.2\text{-}20)$$

If we make the substitution

$$2I_b = 2I_b+\beta V_{in}^2/4 \qquad (2.2\text{-}21)$$

then (2.2-20) reduces to the completely linear transfer function

$$I = V_{in}\sqrt{2\beta I_b} \qquad (2.2\text{-}22)$$

A circuit that can be used to generate the bias current $2I_b+V_{in}^2\beta/4$ is shown in figure 2.2-11.

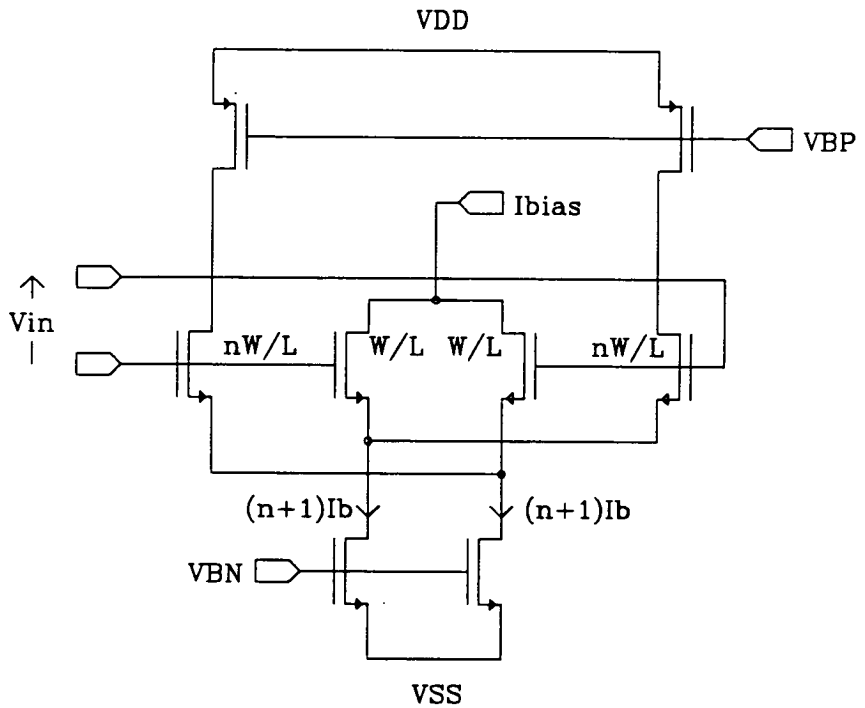


Figure 2.2-11 Circuit to generate bias for adaptively biassed LTP

The current produced by this circuit, I_{bias}, is the sum of the output currents from two asymmetric LTPs. Within each LTP the aspect ratios of the input devices differ by a factor n and the bias current is $(n+1)I_b$. The values of β and I_b referred to here are the same as those in the LTP to be linearised. Using the simple drain current equation (B-3) for each input device the transfer function of the circuit in figure 2.2-11 is found to be

$$I_{bias} = 2I_b + \beta\frac{n(n-1)}{(n+1)^2}V_{in}^2 \qquad (2.2\text{-}23)$$

This equation agrees with (2.2-21) if $n = 1+2\sqrt{3} \cong 2.155$.

A complete adaptively biassed LTP transconductor is shown in figure 2.2-12. The LTP is composed of transistors M_1-M_3 and the bias current is generated by M_3-M_9. M_{10} levelshifts the bias current to the sources of M_1 and M_2.

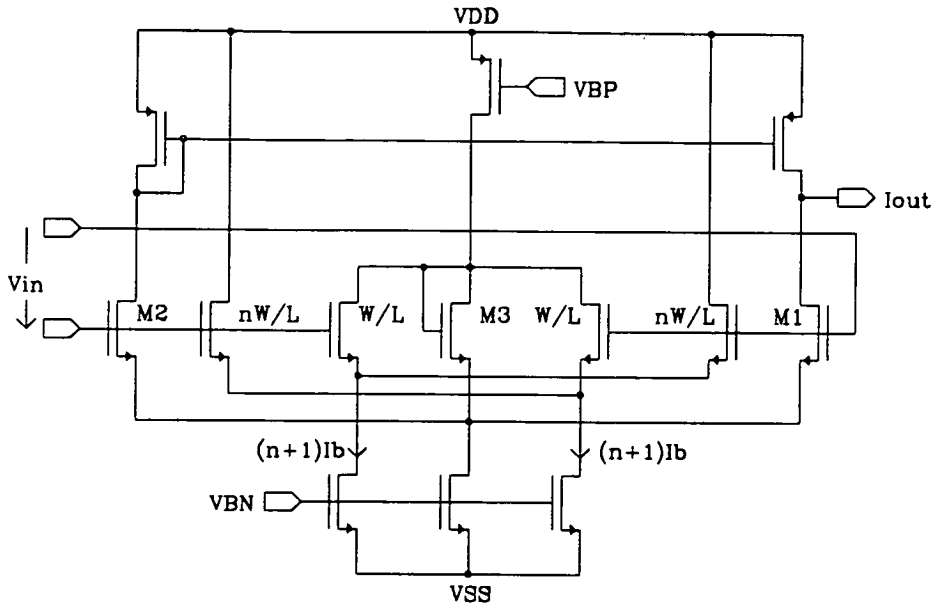


Figure 2.2-12 Complete adaptively biassed LTP transconductor

An undesirable feature of this circuit is that the output is single-ended, the difference between the drain currents of M_1 and M_2 being formed by the simple p-type current mirror M_{13}-M_{14}. The reason for this is that even for a purely differential input voltage a large common mode current is produced, which cannot be cancelled easily by a common mode feedback circuit. This problem is also encountered in some of the saturation mode transconductors described in the next section. It is possible to design high gain CMFB circuits but to be effective the feedback configuration must have a bandwidth much greater than that of the transconductor itself. This presents a serious limit to the frequencies at which such tranconductors may be operated.

2.3 CMOS saturation mode transconductors

A number of transconductance cells have been proposed which attempt to exploit directly the quadratic characteristic of the MOSFET in saturation mode. Whilst differing greatly in detail these circuits are all based on the same basic principle, which we describe with reference to figure 2.3-1.

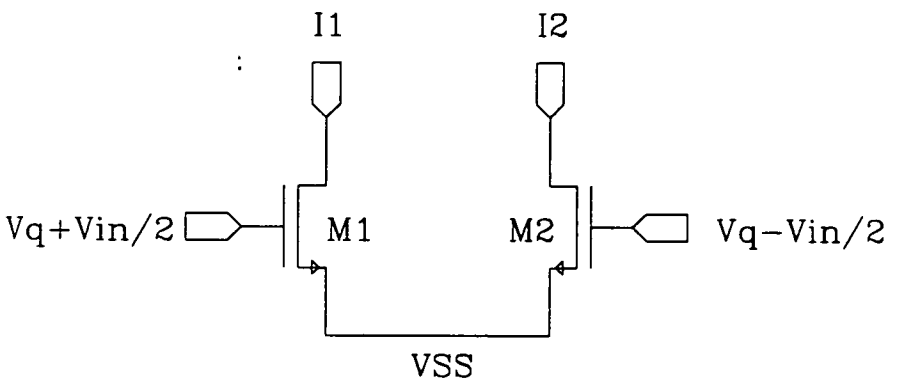


Figure 2.3-1 Pair of MOSFETs in saturation mode

M_1 and M_2 are identical transistors, each of which has a quiescent gate-source voltage V_q. If a signal $+/-V_{in}/2$ is superposed upon the gate-source voltages with opposing polarity then, applying (B-3), the two drain currents can be written:

$$I_1 = 0.5\beta(+V_{in}/2+V_q-V_t)^2 \qquad (2.3\text{-}1)$$

$$I_2 = 0.5\beta(-V_{in}/2+V_q-V_t)^2. \qquad (2.3\text{-}2)$$

If the difference between these two currents is taken, the terms of even order in V_{in} cancel and a linear transconductance is obtained:

$$I_1-I_2 = \beta(V_q-V_t)V_{in}. \qquad (2.3\text{-}3)$$

In principle a very simple transconductor can be obtained by connecting the sources of both M_1 and M_2 to the negative supply and applying V_{in} differentially to the gates, superposed upon the bias voltage V_q. This does give a linear transconductance but suffers from the fact that there is no degree of freedom with which to control the transconductance. A more sophisticated arrangement [33] is illustrated in figure 2.3-2.

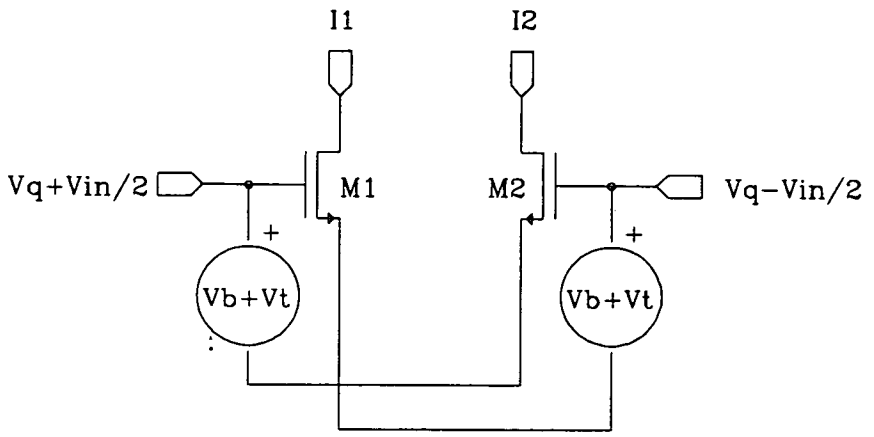


Figure 2.3-2 Controllable saturation mode CMOS transconductance cell

The signal V_{in} is now applied to the gates *and* the sources of the input devices. The quiescent voltage of the sources is held (V_b+V_t) lower than that of the gates by a pair of levelshifters, where V_b is a variable bias voltage. The drain currents of M_1 and M_2 can now be written:

$$I_1 = 0.5\beta(+V_{in}+V_b)^2 \qquad (2.3\text{-}4)$$

$$I_2 = 0.5\beta(-V_{in}+V_b)^2 \qquad (2.3\text{-}5)$$

and their difference is:

$$I_1-I_2 = \beta V_b V_{in} \qquad (2.3\text{-}6)$$

The problem encountered in developing a practical circuit from figure 2.3-2 is the fact that the levelshifters have to accept the currents I_1 and I_2 whilst maintaining a constant value of V_b. Normally a source follower would be used to implement such a variable levelshifter, but in this case the aspect ratio and bias current of the follower would need to be very large to minimise modulation of V_b by the signal current. An ingenious solution to this problem is to replace each input device by a complementary pair [35] such as that shown in figure 2.3-3.

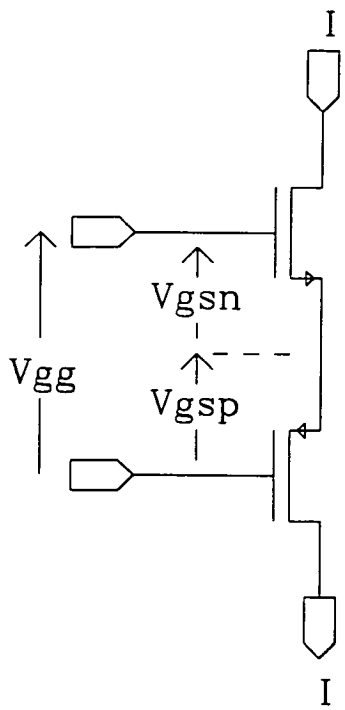


Figure 2.3-3 Complementary CMOS pair

The common drain current can be expressed respectively for the N and P devices as:

$$I = 0.5\beta_n(V_{gsn}-V_{tn})^2 \qquad (2.3\text{-}7)$$

$$I = 0.5\beta_p(V_{gsp}-V_{tp})^2. \qquad (2.3\text{-}8)$$

These two equations can be combined to give:

$$I = 0.5\beta_{np}(V_{gg}-V_{tnp})^2 \qquad (2.3\text{-}9)$$

where

$$\beta_{np} = \frac{\beta_n\beta_p}{(\sqrt{\beta_n}+\sqrt{b_p})^2} \qquad (2.3\text{-}10)$$

$$V_{tnp} = V_{tn}+|V_{tp}| \qquad (2.3\text{-}11)$$

and

$$V_{gg} = V_{gsn}+|V_{gsp}|. \qquad (2.3\text{-}12)$$

The transfer function of the pair (2.3-9) has exactly the same form as that of a single

transistor but now the controlling voltage V_{gg} is applied between two gates. If each input device in figure 2.3-2 is replaced by a CMOS pair as shown in figure 2.3-4, the levelshifters no longer need to supply current, therefore a linear transconductance can be obtained without the use of excessive bias currents.

A complete transconductor using this technique is shown in figure 2.3-4, in which each levelshifter is also implemented as a CMOS pair. It is interesting to note that this transconductance cell was originally proposed as the input stage of a class AB amplifier for switched capacitor circuits [26]; its property of good linearity was noticed several years later [35].

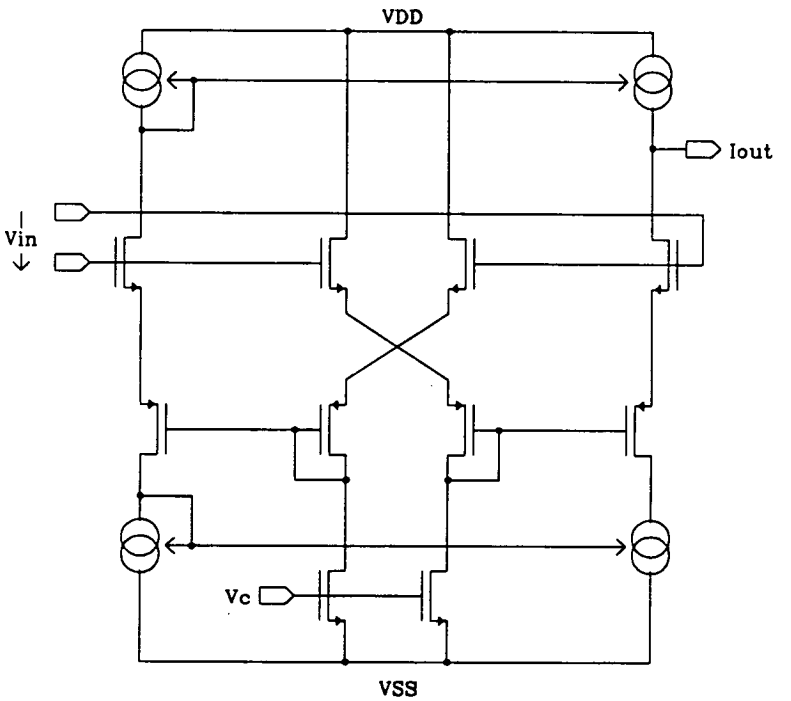


Figure 2.3-4

Transconductor exploiting square law properties of the CMOS pair (figure 2.3-3)

Unfortunately the circuit of figure 2.3-4 is not suitable for application in a high frequency filter in the process used in this project. Firstly there would not be sufficient headroom in a 5V process for the transistor chains which include two gate-source voltages in series. Secondly, as in the case of the adaptively biassed long tail pair, the currents I_1 and I_2 have a common mode component proportional to the square of the *differential* input. This seriously complicates the design of a common mode feedback circuit and in figure 2.3-4 a current mirror is used instead to perform the current subtraction, giving a single-ended output. As previously stated, the use of fully differential signals is desirable in a high frequency filter whereas the presence of current mirrors is not.

It is possible to exploit the square law characteristic of the MOSFET in saturation and avoid the second of the problems desribed above by using the circuit [36,37] shown in figure 2.3-5.

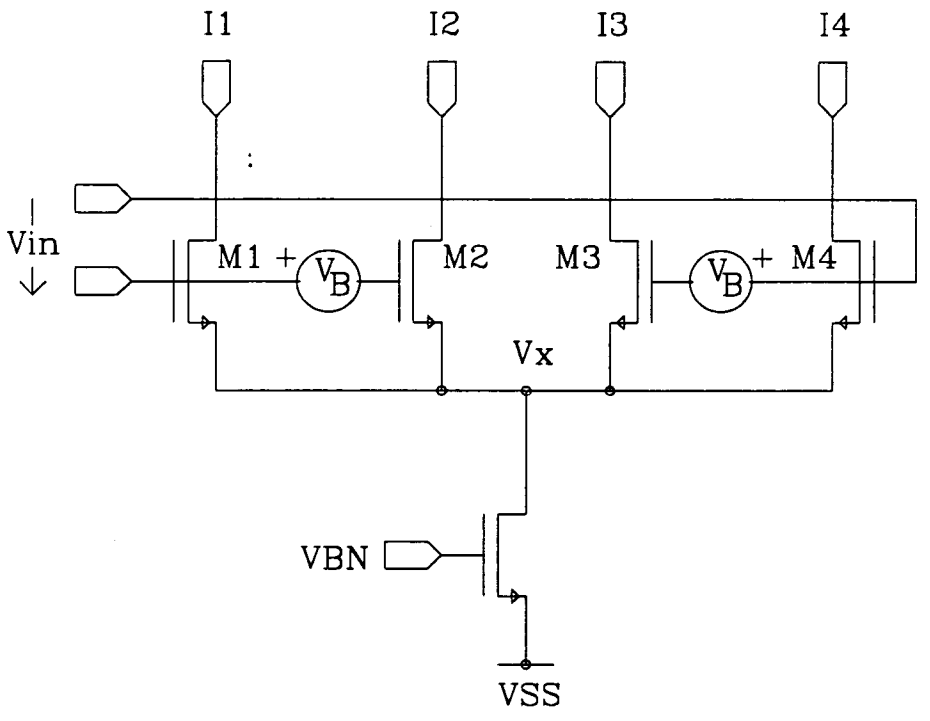


Figure 2.3-5 Saturation mode transconductor with low common mode output

Applying (B-3) again, the drain currents of transistors M_1 to M_4 are written:

$$I_1 = 0.5\beta[V_{in}/2-V_x-V_t]^2 \quad (2.3\text{-}13)$$

$$I_2 = 0.5\beta[V_{in}/2-V_B-V_x-V_t]^2 \quad (2.3\text{-}14)$$

$$I_3 = 0.5\beta[-V_{in}/2-V_x-V_t]^2 \quad (2.3\text{-}15)$$

$$I_4 = 0.5\beta[-V_{in}/2-V_B-V_x-V_t]^2. \quad (2.3\text{-}16)$$

The output current is taken as:

$$I_{out} = (I_1+I_4)-(I_2+I_3) = \beta V_B V_{in} \quad (2.3\text{-}17)$$

which has the desired linearity. The transconductance is controlled by the bias voltage V_B. The levelshifters that provide V_B can be simple source followers, and as in the circuit of figure 2.3-4 they do not have to source or sink any appreciable current. The common mode output current of figure 2.3-5 has a constant value:

$$I_{cm} = (I_1+I_4)+(I_2+I_3) = 2I_b. \quad (2.3\text{-}18)$$

This circuit shares the excellent common mode performance of the simple LTP transconductor described in the previous section. However it would be difficult to use within the headroom of a 5V process due to the presence of gate-source voltages in series (e.g. V_B and V_{gs2}).

The saturation mode transconductors described so far in this section have been developed to capitalise on the high degree of linearity that can be obtained from the square law characteristic. They succeed in this aim and can offer signal swings of several volts with distortion below 1%. However there is a second class of saturation mode transconductors which have been developed for optimum high frequency performance. These are based on the CMOS inverter which has very high frequency parasitic poles due to the absence of internal nodes.

Consider the inverter shown in figure 2.3-6. We define the common gate voltage as a signal V_{in} superposed upon the quiescent voltage V_q at which the currents in the two transistors are equal.

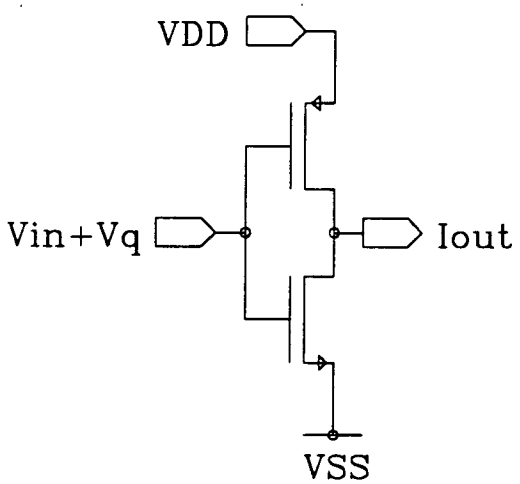


Figure 2.3-6 CMOS inverter

The currents in the n and p devices are respectively:

$$I_n = 0.5\beta_n(V_{in}+V_q-V_{tn})^2 \quad (2.3\text{-}19)$$

$$I_p = 0.5\beta_p(V_{dd}-V_{in}-V_q-V_{tp})^2. \quad (2.3\text{-}20)$$

The output current of the inverter is found by taking the difference between (2.3-19)

and (2.3-20) and eliminating V_q:

$$I_{out} = I_p - I_n = 0.5(\beta_p - \beta_n)V_{in}^2 - \sqrt{\beta_p \beta_n}(V_{dd} - V_{tn} - V_{tp})V_{in}. \qquad (2.3\text{-}21)$$

The transconductance of the inverter has a linear term which can be adjusted in operation only by V_{dd}, so this should be considered a control rather than supply voltage. Unfortunately the second order term of the transconductance will not cancel out unless β_n and β_p are equal. This is not a viable design condition due to the unpredictability of K' factors. A further reason why the simple inverter would not make a good transconductor is that it has very little power supply rejection. What is required is a means of increasing the linearity and PSR without compromising the high frequency performance of the inverter.

One means of satisfying these requirements is to form a fully differential transconductor from two inverters [38,39], shown as Inv_1 and Inv_2 in figure 2.3-7. The symmetry of this configuration removes the even order terms of the transconductance and improves the power supply rejection to an extent determined by the accuracy with which the inverters are matched.

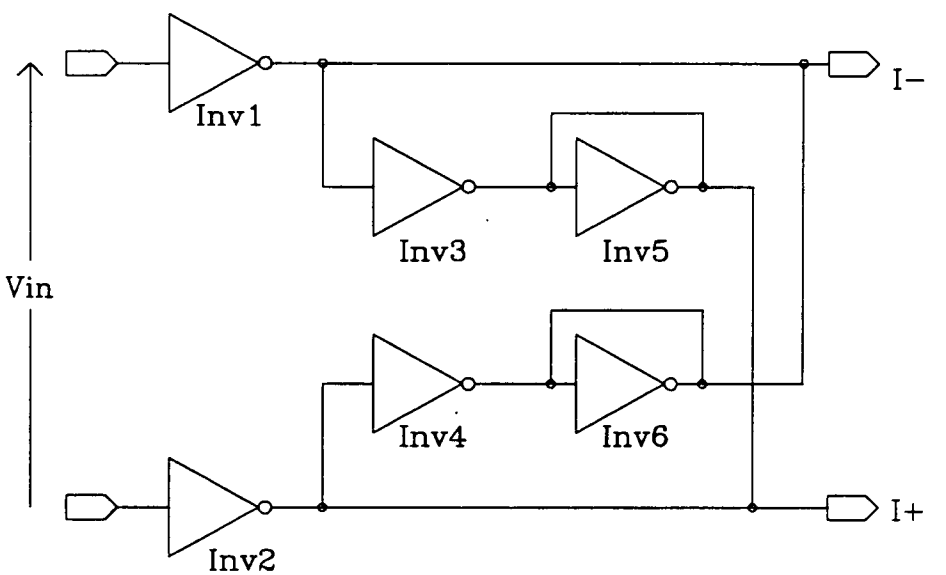


Figure 2.3-7 Transconductor constructed from inverters

For a differential input V_{in} the nominal transconductance is

$$gm = 0.5\sqrt{\beta_p \beta_n}(V_{dd} - V_{tn} - V_{tp}). \qquad (2.3\text{-}22)$$

The other inverters in this figure, Inv_3 to Inv_6, form a load which has low impedance for common mode signals and high impedance for differential signals. This provides common mode stability without a feedback loop, which makes this circuit very promising for vhf application. By adjusting the relative sizes and bias voltages of the load inverters their combined differential conductance can be made negative, with magnitude equal to the output conductance of Inv_1 and Inv_2. The output impedance of the transconductor then appears infinite, making it suitable for use in a high Q filter.

A second means of improving upon the linearity and power supply rejection of the simple inverter is to replace each transistor with the CMOS pair which was introduced in figure 2.3-3. This gives the single ended transconductor [16,40] shown in figure 2.3-8. The second order distortion term is very small for this circuit since it is now determined by the cancellation of the β_{np} values of the upper and lower pairs, rather than by the cancellation of β_n and β_p. The β_{np} values, given by (2.3-10), can be made equal simply by sizing the transistors of like polarity equally. The power supply rejection of this circuit is good, in spite of it being fully single ended, because the outer transistors of the chain are both connected as source followers.

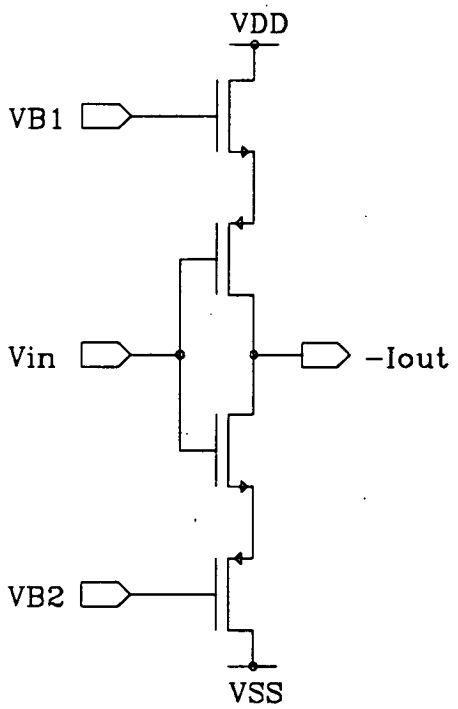


Figure 2.3-8 Inverter transconductor using CMOS pairs

2.4 CMOS triode mode transconductors

The standard equation (B-9) used to predict the channel current of a MOSFET biassed in triode mode indicates that it is linear in the gate-source voltage. This is a very promising observation since it implies that a linear transconductance could be obtained even without cancellation techniques, by holding the drain source voltage of a MOSFET at a low constant value and superposing the input signal upon its gate source voltage.

In practice a differential structure is still desirable to maximise power supply rejection and cancel even order distortion terms, the most significant of which is likely to be that due to the modulation of carrier mobility by the gate-source voltage. Therefore we start by examining the pair of transistors in triode mode, shown in figure 2.4-1.

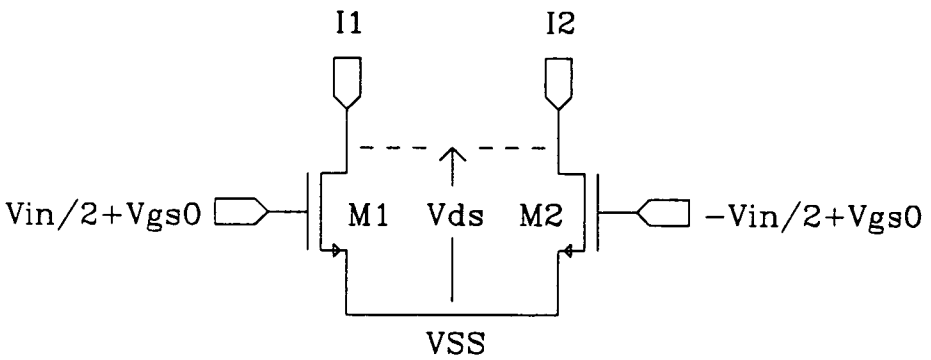


Figure 2.4-1 Pair of MOSFETs in triode mode

Both sources are assumed to be connected to the negative supply and both drain-source voltages are held at the constant value V_{ds}. An input V_{in} is superposed differentially upon the quiescent gate-source voltage V_{gso}, so the drain currents given by (B-9) are (with $\delta = 0$)

$$I_1 = \beta[(+V_{in}/2+V_{gso}-V_t)V_{ds}-V_{ds}^2] \qquad (2.4\text{-}1)$$

$$I_2 = \beta[(-V_{in}/2+V_{gso}-V_t)V_{ds}-V_{ds}^2]. \qquad (2.4\text{-}2)$$

If such a pair forms the input of a fully differential transconductor, the output current will be

$$I_{out} = (I_1-I_2)/2 = 0.5\beta V_{ds}V_{in}. \qquad (2.4\text{-}3)$$

As well as having a perfectly linear ideal response, this configuration is relatively

insensitive to the usual non-ideal effects. For example, the body effect does not operate since the drain and source potentials are held constant.

According to (2.4-3), the value of the triode transconductor is directly proportional to V_{ds}. It is necessary that this voltage be adjustable by a supplied control voltage and that it be independent of the signal in the transconductor. Both of these requirements are met by the configuration [20,41] shown in figure 2.4-2, two of which would be present in a complete transconductor.

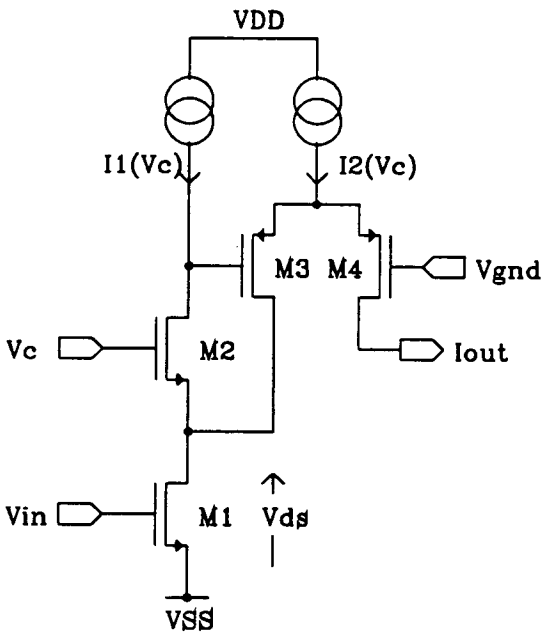


Figure 2.4-2 Circuit to maintain constant V_{ds} of MOSFET in triode mode

The drain-source voltage of the triode device M_1 is set by V_c via the levelshifting action of M_2. M_3, M_4 and the current source I_2 form a folded cascode structure which transfers the signal current from M_1 to a high impedance output. The V_{ds} of M_1 is held constant by a negative feedback loop formed by M_2 and M_3; the operation of which can be described qualitatively as follows. If V_{ds1} tends to increase, this tendency is amplified positively by the common gate amplifier (M_2,I_1) so that the gate voltage of M_3 rises. This causes the proportion of I_2 reaching M_1 to be reduced, which in turn opposes the original increase in V_{ds1}. Since the negative feedback amplifier has two stages its gain can be made large enough to reduce the a.c. component of V_{ds1} to a very small value. However even if V_{ds1} does contain a component proportional to V_{in} this will cause a term proportional to V_{in}^2 in the drain current which will be cancelled significantly by the corresponding term in the other half of the fully differential circuit.

If a filter is designed with closed loop integrators (as defined in section 1.2), extremely simple triode mode transconductors can be used [42,43]. An example of these are the so-called "MOSFET-C" circuits [44,45]. The basic principle applied is to adapt conventional RC circuits by replacing each resistor with a MOSFET channel. The values of the MOSFET resistors can be adjusted by the gate bias, and the non-linearities of the transistor characteristic are cancelled by the use of fully-balanced and cross-coupled circuits. MOSFETs are similarly used as variable resistors in the degenerated long tail pair transconductors described in section 2.2 and the variable phase transconductor described in chapter 5.

The basic MOSFET-C integrator is illustrated in figure 2.4-3. We assume the inputs of the amplifier to be virtual earths at signal ground. The currents in M_1 and M_2 are then given by (B-9) as:

$$I_1 = \beta[+(V_c-V_t)V_{in}/2-V_{in}^2/4] \quad (2.4\text{-}4)$$

$$I_2 = \beta[-(V_c-V_t)V_{in}/2-V_{in}^2/4], \quad (2.4\text{-}5)$$

and the differential output voltage is

$$V_{out} = V_{in}\beta(V_c-V_t)/sC. \quad (2.4\text{-}6)$$

So a linear integrator is achieved whose time constant can be controlled by the MOSFET gate voltage V_c. I_1 and I_2 also have a common mode component proportional to $V_{in}/2$. This would induce a corresponding component in V_{out} if it were not for the common mode feedback loop which must be included within the amplifier. The effect of the CMFB in the opamp of the MOSFET-C integrator is to make the voltage of the amplifier inputs an even ordered function of V_{in}, such that very little common mode current is actually produced in M_1 and M_2.

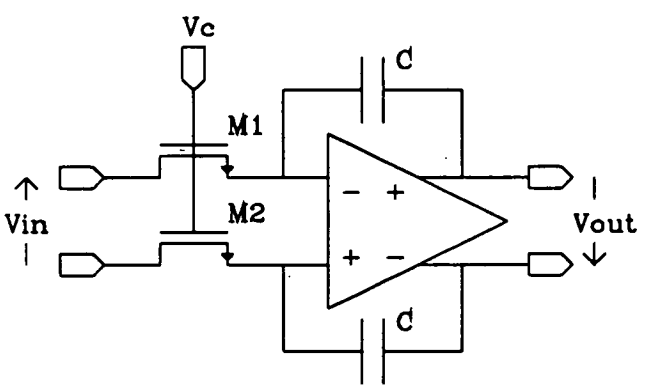


Figure 2.4-3 Two transistor MOSFET-C integrator

A MOSFET-C integrator with improved performance is obtained by cross-coupling two identical transistor pairs, as shown in figure 2.4-4. The transfer function of this integrator is:

$$V_{out} = V_{in}\beta(V_{c1}-V_{c2})/sC. \qquad (2.4\text{-}7)$$

This transfer function is independent of the threshold voltage, as long as it is the same for each device, and hence does not suffer from distortion due to the body effect. Theoretically this circuit cancels distortion terms of any order, in contrast to the integrator with two input transistors which only cancels the even terms. In both circuits the cancellation depends upon the accuracy with which the β values of the input transistors are matched. Equation (2.4-7) demonstrates a very linear multiplication of the two differential voltages, V_{in} and $(V_{c1}-V_{c2})$, and this feature has been exploited in a radio frequency quadrature detector circuit [46].

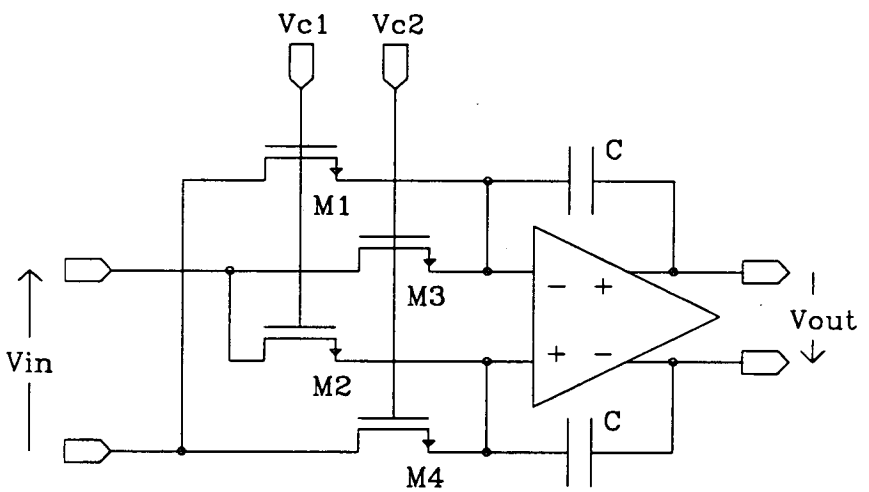


Figure 2.4-4 Four transistor MOSFET-C integrator

2.5 Other FET transconductors

In addition to the many CMOS transconductor designs to be found in the literature, a few exist in other FET technologies [47,48,49]. Some of these are now of historical interest whereas some have potential for the future. The characteristics of different types of FET (NMOS, PMOS, JFET, GaAs MESFET) are similar, showing a square law behaviour in saturation and a threshold (or "pinch-off") value of gate-source voltage required for significant conduction. This fact might suggest that the CMOS transconductor circuits described in the previous three sections could be transported easily to the other FET technologies. However this transportation is not always direct, due to the fact that CMOS uses complementary enhancement devices whereas the other technologies use depletion devices to a large extent.

The basic transconductor filter architecture, employing a phase lock loop for tuning, was in fact first presented in a JFET/Bipolar technology by Tan and Gray [48] in 1977. They did not integrate a complete filter, but breadboarded a ladder filter from individual integrators. The integrator circuit is illustrated in figure 2.5-1.

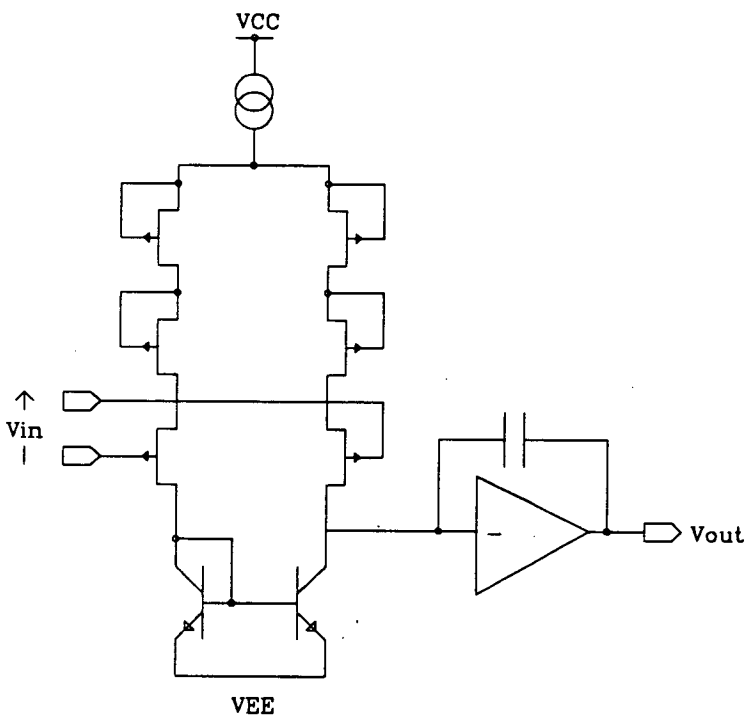


Figure 2.5-1 JFET integrator

The voltage to current conversion is effected by a long tail pair with JFET input devices and bipolar active loads. The JFETs exhibit a square law characteristic similar to that of MOSFETs therefore the linearity of a JFET LTP is generally as poor as that of a CMOS LTP. In figure 2.5-1 the linearity is improved by using additional

diode connected JFETs to degenerate the input stage. The current from the input stage is fed into a Miller capacitor connected around a high gain stage to complete the integrator (i.e. this is a closed loop integrator). The time constant is controlled by adjusting the long tail bias current.

Integrated analogue filters operating at very high frequencies may be produced in future using Gallium Arsenide (GaAs) technology. GaAs circuits are capable of very high frequency operation due their high electron mobility (approximately six times the mobility in silicon) and the low parasitic capacitances associtated with the insulating substrate. Experimental GaAs switched capacitor filters have already been fabricated [11] and possible GaAs transconductor circuits are being investigated.

One such ciruit is shown in figure 2.5-2, in which the four transistors are identical MESFETs [49]. This relies on the square law cancellation technique introduced with respect to CMOS circuits in section 2.3.

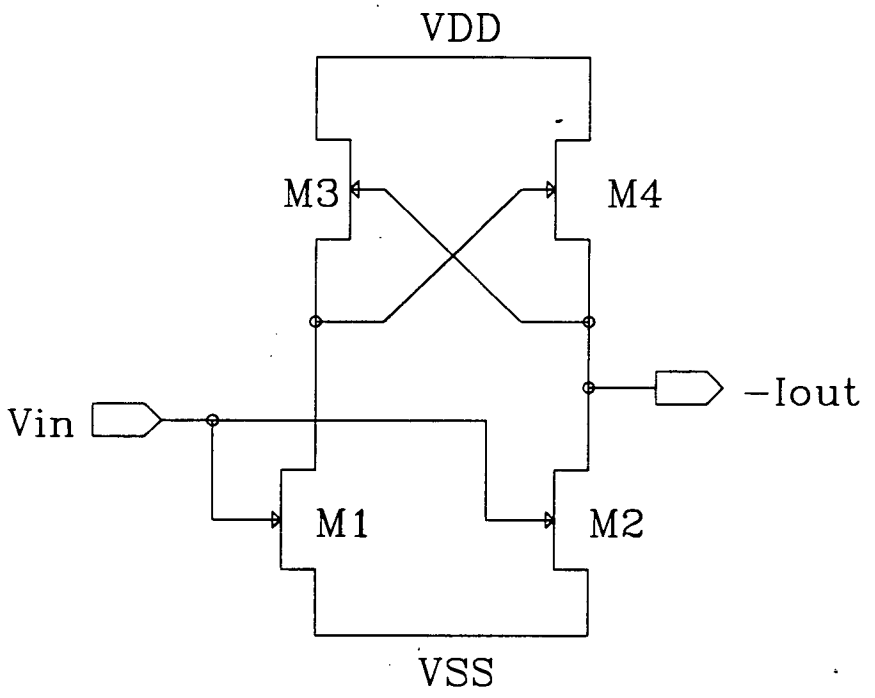


Figure 2.5-2 GaAs MESFET transconductor

The drain currents of the grounded transistors are given by

$$I_1 = I_2 = 0.5KW[V_{in}-V_t]^2, \qquad (2.5\text{-}1)$$

where K, V_t and W represent gain factor, threshold voltage and channel width

respectively. The drain currents of M_1 and M_3 are equal so the gate-source voltage of M_3 must also equal V_{in}. Since the inputs to M_3 and M_4 are cross connected the current in M_4 is therefore

$$I_4 = 0.5KW[-V_{in}-V_t]^2, \tag{2.5-2}$$

and the output current of the transconductor is

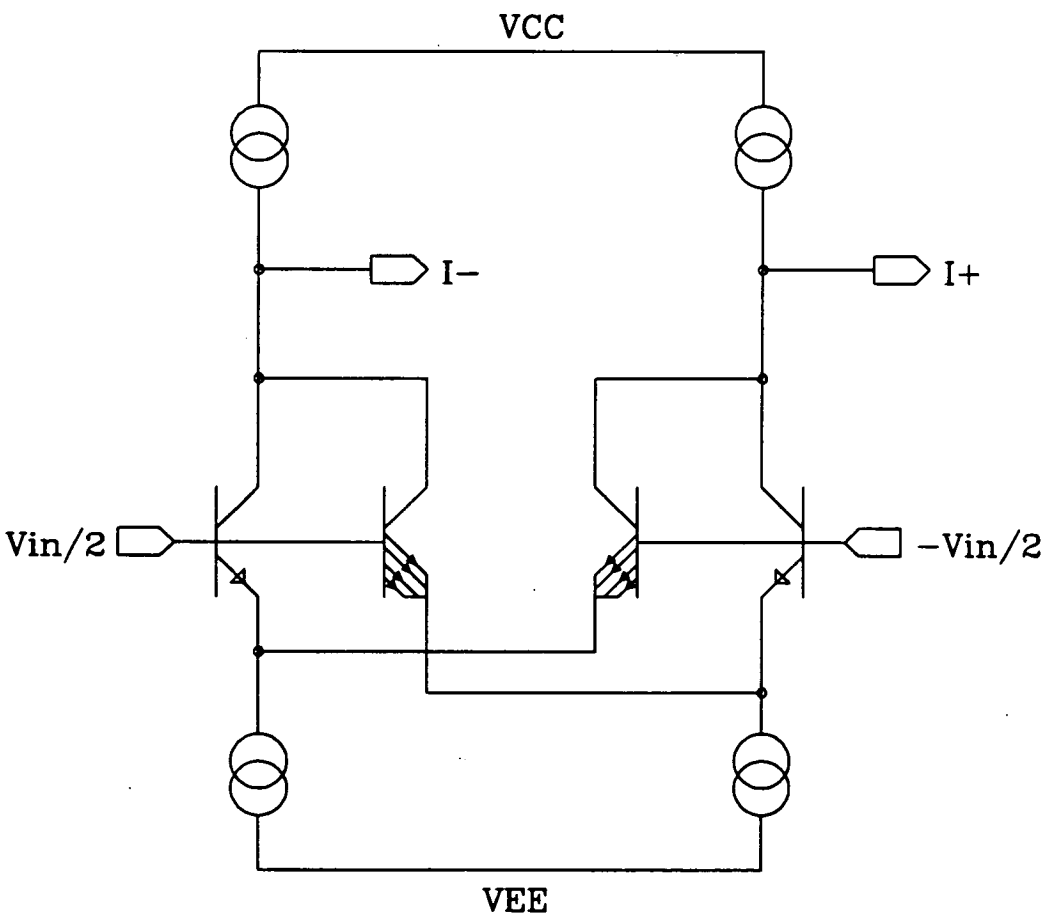
$$I_{out} = I_4-I_1 = -2KWV_tV_{in}, \tag{2.5-3}$$

so the transfer function is linear to the accuracy of the square law model. The two obvious disadvantages of this transconductor as it stands are that the transconductance is not tunable and the power supply rejection is likely to be poor since the input signal is defined by V_{in}-V_{ss} with no cancellation mechanism. Both problems can probably be overcome by incorporating one or more of the cell shown in a more sophisticated circuit.

2.6 Bipolar transconductors

The application of bipolar transistors to transconductor design [50,51,52,53,54,55] is fundamentally different to that of FETs for two reasons. Firstly, the exponential characteristic of bipolar transistors makes them less amenable to the use of simple cancellation schemes for linearisation, which are easily applicable to the quadratic characteristics of FETs. Secondly, it is hard to make a bipolar transconductor approximate to the requirement for infinite input impedance due to base bias current. For this reason the output of each integrator in a bipolar filter is usually buffered before application to the inputs of other integrators, or alternatively closed loop integrators are used which have low output impedance capable of driving base inputs.

The bipolar LTP is much less linear than the CMOS LTP and could only be used as a transconductor for very small signals (tens of mV). As in the CMOS case the range can be extended by cross-coupling non-identical LTP's. Figure 2.6-1 shows such a circuit in which each of the two LTP's has a 4:1 ratio in emitter area between its two input devices [53].



A less crude way of achieving linear transconductance is to adapt well established bipolar multiplier circuits, such as the Gilbert multiplier. As an example we consider the integrator circuit shown in figure 2.6-2.

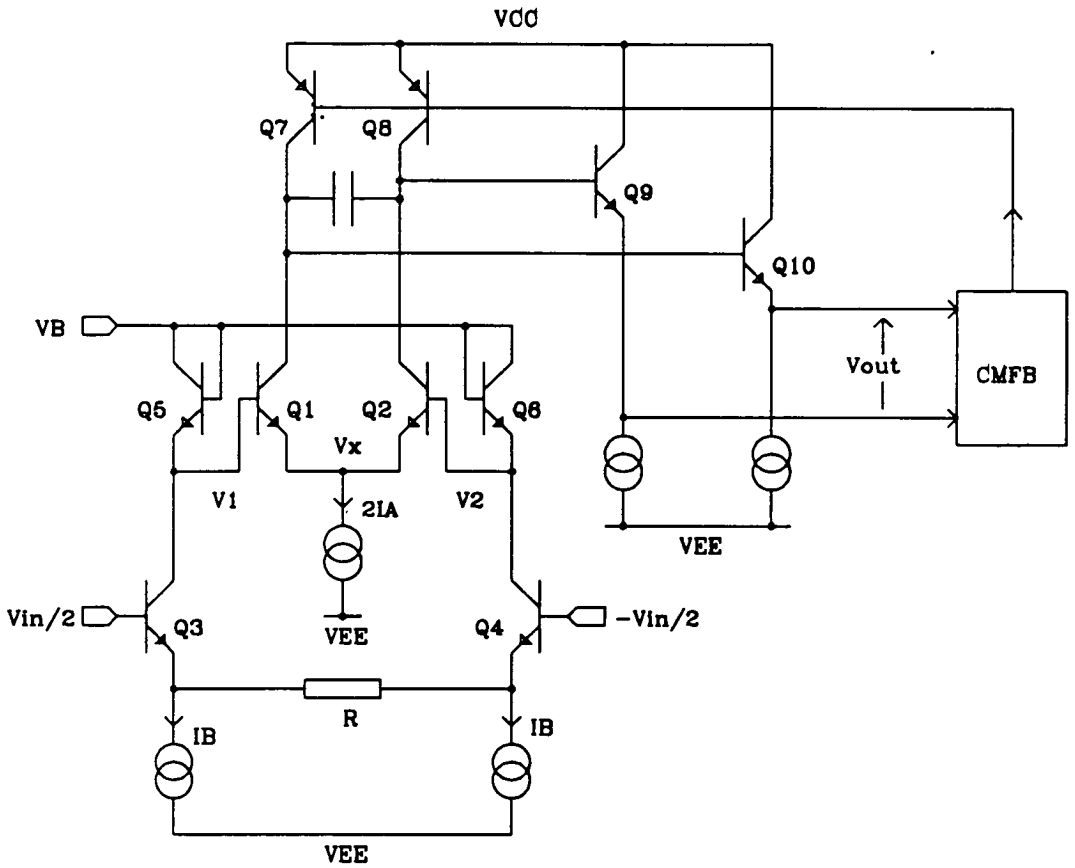


Figure 2.6-2 Bipolar integrator

The core of the circuit is the differential pair consisting of Q_1 and Q_2. Applying equation (B-10) and using the notation shown in the figure, the collector currents of Q_1 and Q_2 can be written:

$$I_1 = I_S \exp[(V_1 - V_X)/V_T] \qquad (2.6\text{-}1)$$

and

$$I_2 = I_S \exp[(V_2 - V_X)/V_T]. \qquad (2.6\text{-}2)$$

V_X is eliminated by dividing (2.6-1) by (2.6-2) to give

$$I_1/I_2 = \exp[(V_1 - V_2)/V_T] \qquad (2.6\text{-}3)$$

The following expression for the output current of the differential pair is obtained applying using (2.6-3) and assuming that the current gains of Q_1 and Q_2 are sufficiently high to justify the relation $I_1+I_2=2I_A$:

$$(I_1 - I_2)/2 = I_A \tanh[(V_1 - V_2)/2V_T]. \qquad (2.6\text{-}4)$$

Equation (2.6-5) approximates to a linear function only if the argument of the tanh function is much less than unity. To achieve a linear transconductance for large signals we require:

$$V_1 - V_2 = 2V_T \tanh^{-1}(\alpha V_{in}). \qquad (2.6\text{-}5)$$

where α is a parameter with the dimensions of inverse voltage.

The inverse tanh function is realised by Q_3-Q_6 and R_1. The resistor degenerates Q_3 and Q_4 so that

$$(I_3 - I_4)/2 = V_{in}/R_1. \qquad (2.6\text{-}6)$$

This equation relies on the assumption that the transconductance of the transistors is much greater than the conductance of the resistors, and that the base currents are negligible compared to the collector currents. Q_5 and Q_6 form a diode connected pair connected to the bias voltage V_B. Applying (B-10) and the approximation $I_3+I_4=2I_B$, their large signal differential resistance is found to be the inverse of the transconductance of Q_1 and Q_2, therefore

$$V_1 - V_2 = 2V_T \tanh^{-1}[V_{in}/I_B R_1] \qquad (2.6\text{-}7)$$

Substituting (2.6-7) into (2.6-4) we obtain the transconductance equation

$$(I_1 - I_2)/2 = V_{in}[I_A/R_1 I_B]. \qquad (2.6\text{-}8)$$

The transconductance can be controlled in operation by adjusting the ratio of bias currents I_A/I_B. The integrator is completed by a load capacitor, output buffers (Q_9 and Q_{10}) and a common mode feedback circuit. The use of pnp devices is restricted to the active loads (Q_7 and Q_8) since in most bipolar processes they have considerably worse high frequency performance than the npn devices.

CHAPTER 3
REVIEW OF TRANSCONDUCTOR FILTER DESIGN

3.1 Introduction

Transconductor filters have been designed by methods analogous to those used for other active filters. The most popular approach is to derive the active circuit from a passive LC prototype ladder [19,20,24,30]. This can involve the interconnection of integrators to form so called "leapfrog" ladders, or resonators forming "coupled biquad" ladders. An alternative method is to construct the active filter from a series of stages each of which implements up to two poles and two zeros of the desired transfer function [6,16,17,18]. These are called "cascaded biquad" filters, since each stage can individually have a biquadratic transfer function. In general ladder circuits are preferable to cascaded biquads because a passive prototype ladder has a very low sensitivity to component value errors which is carried over to the active circuit [21].

Section 3.2 shows how conventional ladder methods can be applied to the design of transconductor filters. The limitations of conventional ladder circuits are discussed to set the context of the new design methods which are introduced in chapter 6.

Transconductor filters differ from SC filters by their requirement for automatic tuning circuits. The ratios of pole and zero frequencies can be designed accurately in a transconductor filter by the ratios of like component values, but the absolute pole and zero frequencies are not accurately predictable due to the variability and temperature dependence of process parameters, such as MOSFET gain factor and threshold voltage. This implies that without tuning, the shape of the filter response can be designed accurately, but not its scaling in frequency.

The most popular type of automatic tuning is the master-slave system [48], illustrated in figure 3.1-1. This consists of the desired filter (the slave) plus a frequency control loop (the master).

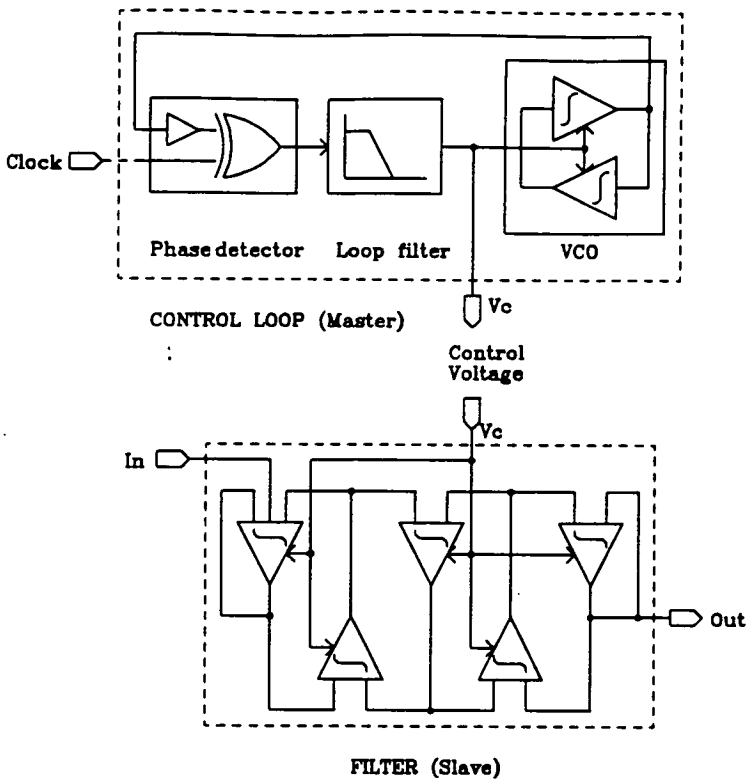


Figure 3.1-1 Master-slave filter tuning system

The control loop circuit is constructed from the same type of transconductor/capacitor integrator as is used in the main filter. Its function is to adjust the transconductance such that the integrator time constant remains in fixed ratio to the period of an externally applied reference clock signal. Within the negative feedback of the loop is a d.c. control voltage, V_C, which monotonically adjusts the transconductance. This control voltage is also applied to each transconductor in the filter as the result of which the filter transfer function is scaled correctly in frequency with respect to the reference clock. The frequency of the reference clock should be chosen, if possible, to lie outside the passband of the filter so that, if any breakthrough occurs, it will not interfere with the signal. This requirement can be hard to meet for high frequency filters. If the filter transfer function contains any transmission zeros, the reference frequency can be chosen to coincide with one of them for maximum rejection.

The success of a master-slave system depends on how well the control loop locks the integrator time constant to the clock period and how well the transconductors in the filter match those in the control loop. The first of these points affects what type of PLL (or other circuit) is used in the control loop. The second affects both the design of the transconductor and the overall layout of the filter. Matching is enhanced by designing as large as possible those transistors which set the value of the transconductor, subject of course to other considerations such as the

parasitic capacitance of these devices. This precaution reduces the effect of random errors arising from inaccuracy in etching. Systematic matching errors can result from gradients in dielectric thickness and doping concentrations across the chip, and from mask misalignment. The effects of these errors are minimised respectively by placing all the transconductors to be matched close together and giving them the same orientation.

It is possible to design a control loop which refers the transconductor value to the conductance of a precision resistor instead of a clock reference. This is less satisfactory as it does not compensate for the tolerance in capacitor values, and it will not even set the transconductor values correctly unless the reference resistor has a very low temperature coefficient.

At very high frequencies it is necessary not just to control the frequency response of the filter, but also to compensate for phase errors in the transconductors which can lead to distortion of the transfer function and instability. It is possible to extend the master-slave system to compensate for phase errors by the addition of one or more amplitude lock loops (ALLs) [16]. The design of frequency and phase control systems are discussed in sections 3.3 and 3.4.

3.2 Ladder filters

The first step in the design of any active ladder filter is to obtain a passive prototype which meets the given specification template. Tables are available [59] which list component values for lowpass ladders using standard approximations such as Butterworth, Bessel, Chebyshev and elliptic. Component values for other types of frequency response (bandpass, bandstop and highpass) can be obtained by applying standard frequency transformation and scaling methods [4]. Alternatively, computer programs can be used to generate a passive ladder automatically for more general approximations and any response type [60].

Traditionally two methods have been used to derive an active circuit from a passive prototype ladder. The first ("direct" simulation) involves the substitution of those components which are unavailable (inductors and sometimes resistors) by simulated elements, which are combinations of amplifiers and the available passive components [30,52]. The second method ("operational", "indirect" or "signal flow graph" simulation) involves the representation of selected currents and voltages of the prototype, or algebraic combinations of them, by proportionate voltages in the active circuit [19,48]. Recently, a much more powerful matrix based approach has been developed and applied to the design of SC, RC and digital ladder filters [61,62]. In the case of SC filters this has led to ladder circuits which are far from intuitively obvious but which offer improved performance with respect to parameters such as settling time, capacitance spread and canonicity. In chapter 6 of this thesis the matrix approach is extended to the design of transconductor filters and is shown to lead to new and useful circuit topologies. In the remainder of this section we describe the two established methods and their limitations.

In a transconductor filter the only passive components used are capacitors, therefore in a direct simulation of the prototype simulated elements are required for resistors and inductors. Normally the input to a passive ladder is drawn as a voltage source in series with the termination resistor. However for a transconductor implementation it is clearer to use the Norton equivalent of a voltage controlled current source in parallel with the resistor. For this reason a simulated element is required only for grounded resistors. This is provided simply by connecting the output of a transconductor to its negative input and grounding the positive input, or in the fully differential case, by connecting the outputs to the inputs of opposite polarity. Both of these elements are illustrated in figure 3.2-1. The effective value of the resistor is the reciprocal of the transconductance.

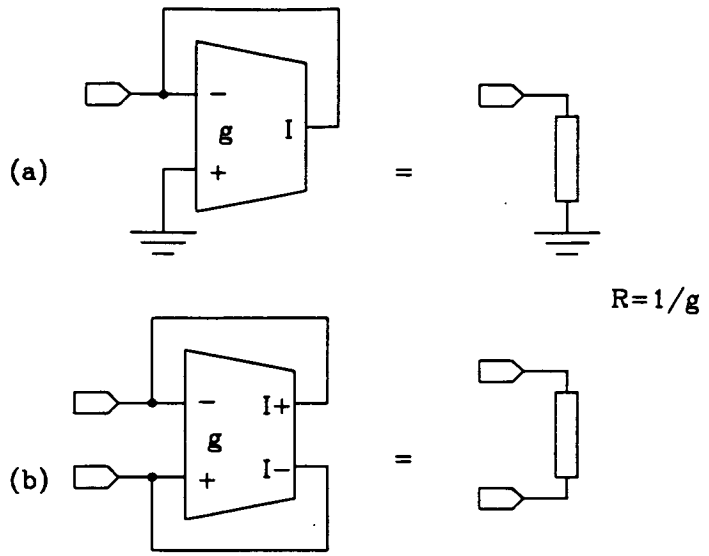


Figure 3.2-1 Simulating a grounded resistor with a transconductor
(a) single ended, (b) fully differential

Simulated inductors, both grounded and floating, are implemented by the use of a construct called the gyrator [4,50] whose symbol is shown in figure 3.2-2. The operation of the gyrator is defined by:

$$I_1 = gV_2 \qquad (3.2\text{-}1a)$$

$$I_2 = -gV_1. \qquad (3.2\text{-}1b)$$

where g is a constant.

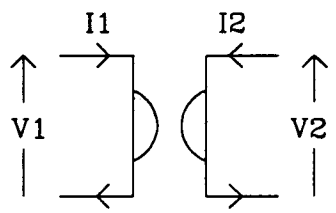


Figure 3.2-2 Symbol for a gyrator

It is evident from these equations that the gyrator can be realised by two transconductors of value g connected back to back with negative loop gain, as shown in figure 3.2-3.

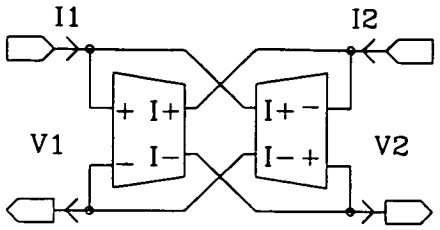


Figure 3.2-3 Gyrator constructed from two transconductors

To simulate a grounded inductor, a capacitor is connected to one side of a gyrator, figure 3.2-4, so that

$$I_2 = -sCV_2. \tag{3.2-2}$$

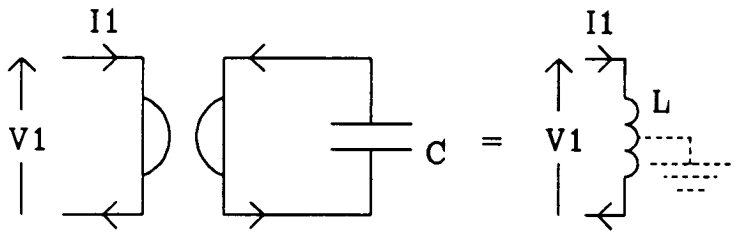


Figure 3.2-4

Simulation of a fully differential grounded inductor using gyrator and a capacitor

Equations (3.2-1) and (3.2-2) are solved to give

$$I_1 = \frac{g^2}{sC}V_1. \tag{3.2-3}$$

By equating coefficients with the equation defining inductance [66], we find that for an inductance of value L, the required capacitor value is

$$C = g^2L. \tag{3.2-4}$$

A floating inductor is implemented by two gyrators and a capacitor as shown in figure 3.2-5, the value of the capacitor again being given by (3.2-4).

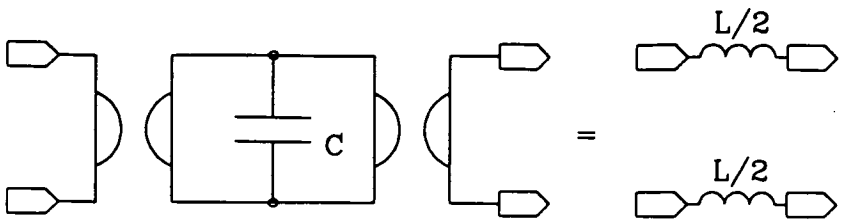


Figure 3.2-5 Simulation of a floating inductor using two gyrators and a capacitor

In the fully differential circuits presented in this chapter, the capacitors connected between the outputs of a transconductor are shown for simplicity as a single component. However in an integrated circuit either two or four capacitors are used, for a number of reasons. Firstly, account must be taken of the parasitic capacitance that exists between the bottom plate and the substrate (or well), which usually has a sheet value approximately 10% of the drawn value. In order to preserve the symmetry of the circuit, a differential load must be composed of two capacitors connected such that there is equal parasitic capacitance on each output node. This arrangement is shown in figure 3.2-6, in which the capacitor bottom plates are identified by fins. In fact the value of each capacitor must be slightly lower than the nominal value (C/2) to allow for the parasitic. A disadvantage of this load is that it has little common mode component, which may be a problem if the common mode feedback circuit of the transconductor requires load compensation.

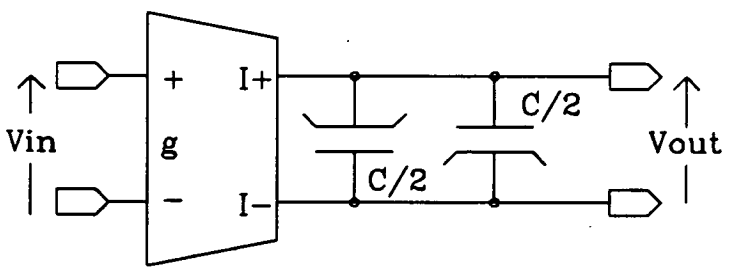


Figure 3.2-6 Practical floating load arrangement

The effect of the bottom plate parasitic can be avoided completely *and* common mode load provided by using two capacitors each of whose bottom plates is connected to ground, as shown in figure 3.2-7. These capacitors are in series for differential signals, so each must have twice the value of the desired load. Therefore this arrangement requires four times the capacitance of the non-grounded version for the same effective load. At low frequencies this may be a problem, but at higher

frequencies it is desirable to maintain higher capacitor values for the benefit of matching. All of the high frequency experimental filters described in chapter 7 use this type of load.

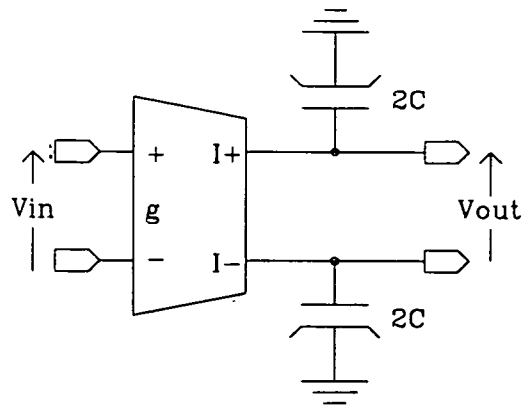


Figure 3.2-7 Practical grounded load arrangement

If it is required to minimise the total capacitance whilst still providing a common mode load, a combination of the floating and grounded loads can be used, as illustrated in figure 3.2-8. The four capacitors give a total differential load C and a common mode load of $2\alpha C$ on each output, where α is a parameter which can take values between 0 and 1. In these two limits figure 3.2-8 reduces to figures 3.2-6 and 3.2-7 respectively. If $\alpha < 1$ then the parasitic of the floating load capacitors must be calculated and subtracted from either the floating or grounded capacitors. The low pass filter reported in reference 20 uses four load capacitors in each integrator with $\alpha=1/3$ as a result of which the total capacitance has half the value it would have if only grounded capacitors were used.

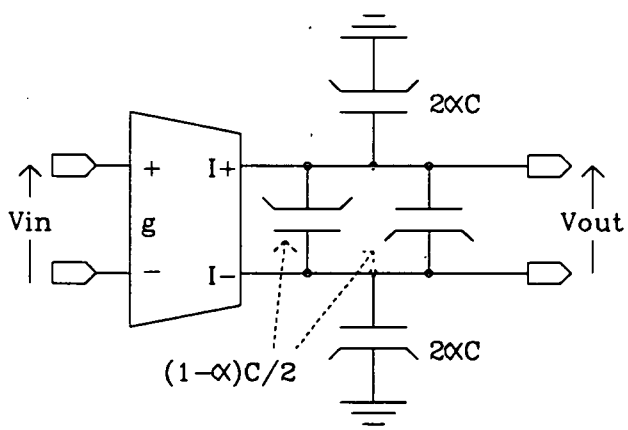


Figure 3.2-8 Differential load of both grounded and floating capacitors

To illustrate direct simulation we consider the prototype ladder shown in figure 3.2-9.

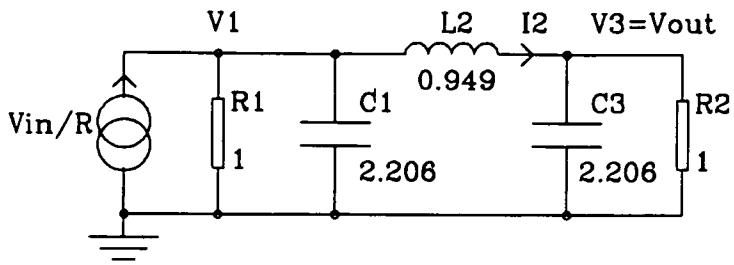


Figure 3.2-9 Third order all-pole lowpass RLC prototype filter

This is a third order lowpass ladder, which can be used to realise all-pole transfer functions such as Butterworth and Chebyshev. The component values marked in the figure give a Chebyshev response with 1.25dB passband ripple, normalised to a cutoff frequency of 1 rad/s. An unscaled active version of this ladder, figure 3.2-10, is obtained by using the simulated resistors and inductors described above with a transconductor value of 1S (i.e. 1Amp/Volt). To obtain a practical circuit three scaling operations must be considered, namely magnitude, frequency and impedance scaling.

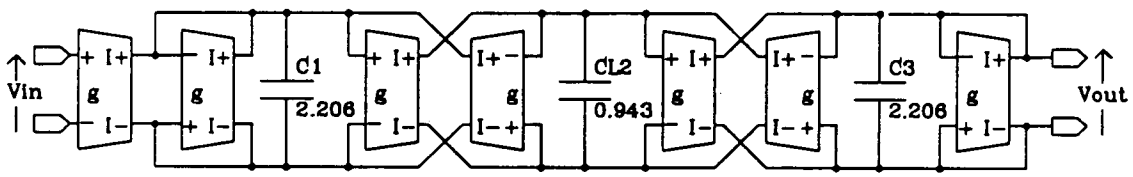


Figure 3.2-10

Unscaled transconductor ladder obtained by direct simulation of figure 3.2-9

The aim of magnitude (or nodal voltage) scaling is to make sure that the peak values of all voltages within the circuit are reasonably close to each other within the filter passband. This criterion maximises the dynamic range of the filter, and reduces distortion due to excess phase by ensuring that the unity gain frequency of each integrator is close to the filter passband. The most common magnitude scaling operation is to compensate for the 6dB attenuation of the doubly terminated prototype, so that the insertion loss of the filter is 0dB. This is easily done by doubling the value of the input transconductor, which is equivalent to connecting two unit transconductors in parallel. Having done this it is often found that one or more of the internal nodes has a peak voltage amplitude that is not close to 0dB. For

example the voltage across capacitor C_{L2} in figure 3.2-10 has a passband gain of 6dB with respect to the input and a peak value of 12.9dB. This can be reduced by 6dB simply by doubling the value of the capacitor. In order that the overall transfer function of the filter be unaffected by this change, it is necessary to double the values of the transconductances which refer to this voltage as their input.

Prototype ladders obtained from tables are usually normalised to a cutoff frequency of 1rad/sec (≅0.16Hz). The frequency of the active filter can be scaled up from this value by a factor μ, by dividing each capacitor by μ. This operation relies on the fact that every time constant in the transfer function can be expressed as the ratio of a capacitance to a transconductance (where these are combinations of capacitor and transconductor values in the filter).

The same fact allows the impedance of the filter to be scaled without altering its magnitude or frequency response. Impedance scaling involves multiplying all transconductors and capacitors by the a factor, θ, such that they satisfy a number of criteria. Most importantly the values have to be practicably realisable which in current integrated circuit technology means transconductors in the range 1μS to 1mS and capacitors in the range 0.1pF to 100pF. Within these limits, which are of course approximate, it is desirable to lower the impedances as far as possible, i.e. use transconductors and capacitors of large value, in order to minimise thermal noise and component mismatch. The price for large component values is paid in terms of the chip area and current required.

Figure 3.2-11 shows the component values which result from scaling the magnitude, frequency and impedance of the ladder of figure 3.2-10 to give a cutoff frequency of 4MHz (μ=8e6π) and a transconductor impedance of 10kΩ (θ=1e-4). The results of a SPICE a.c. simulation of this filter are shown in figure 3.2-12.

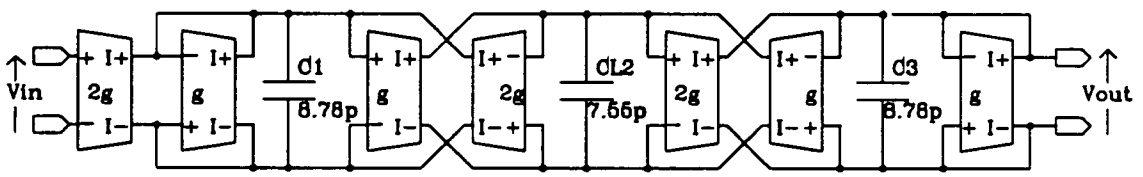


Figure 3.2-11

Lowpass transconductor ladder scaled to 4MHz cutoff frequency, 10kΩ impedance and 0dB insertion loss

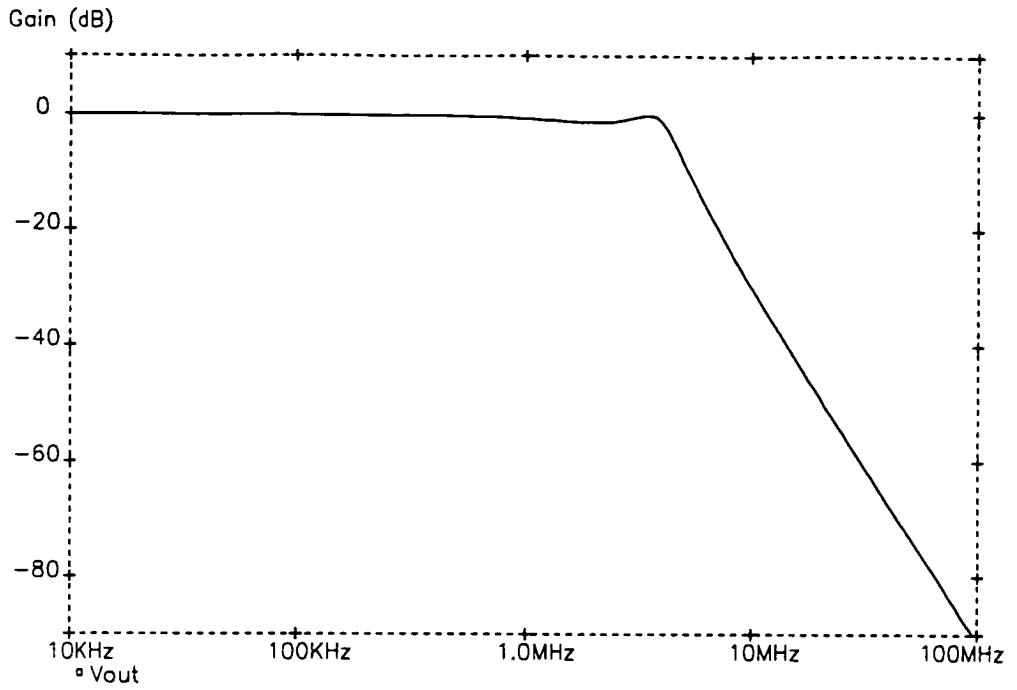


Figure 3.2-12 SPICE simulation of lowpass transconductor ladder (figure 3.2-11)

Now we consider the design of a leapfrog ladder using operational simulation from the same prototype (figure 3.2-9). First, Ohm's law and Kirchhoff's current law are applied to obtain expressions for the voltages across the capacitors and the current in the inductor:

$$V_1 = \frac{1}{sC_1}\left(\frac{V_{in}-V_1}{R}-I_2\right)$$

$$I_2 = \frac{1}{sL_2}(V_1-V_2)$$

$$V_3 = \frac{1}{sC_3}\left(\frac{-V_3}{R}+I_2\right) \qquad (3.2\text{-}5a\text{-}c)$$

Next a variable V_{L2} and the constants C_{L2}, α, n, and g are introduced by the definitions

$$ngV_{L2} = I_2 \qquad (3.2\text{-}6)$$

$$g = \frac{1}{\alpha R} \qquad (3.2\text{-}7)$$

$$C_{L2} = g^2 L_2 \qquad (3.2\text{-}8)$$

Using these definitions, (3.5a-c) can be rewritten

$$V_1 = \frac{g}{sC_1}[\alpha(V_{in}-V_1)-nV_2]$$

$$V_{L2} = \frac{g}{snC_{L2}}[V_1-V_3]$$

$$V_3 = \frac{g}{sC_3}[nV_2-\alpha V_3]. \qquad (3.2\text{-}9a\text{-}c)$$

To form the active circuit, each of (3.2-9a-c) is implemented by a summing integrator, as shown in figure 3.2-13. To scale the voltage across C_{L2} correctly, we set α=1 and n=2. An inspection of figures 3.2-11 and 3.2-13 reveals that the direct and operational simulations of this passive prototype in fact lead to the same active circuit. The circuits appear to be different, but are identical because an N input transconductor is equivalent to N single input transconductors with their output currents summed.

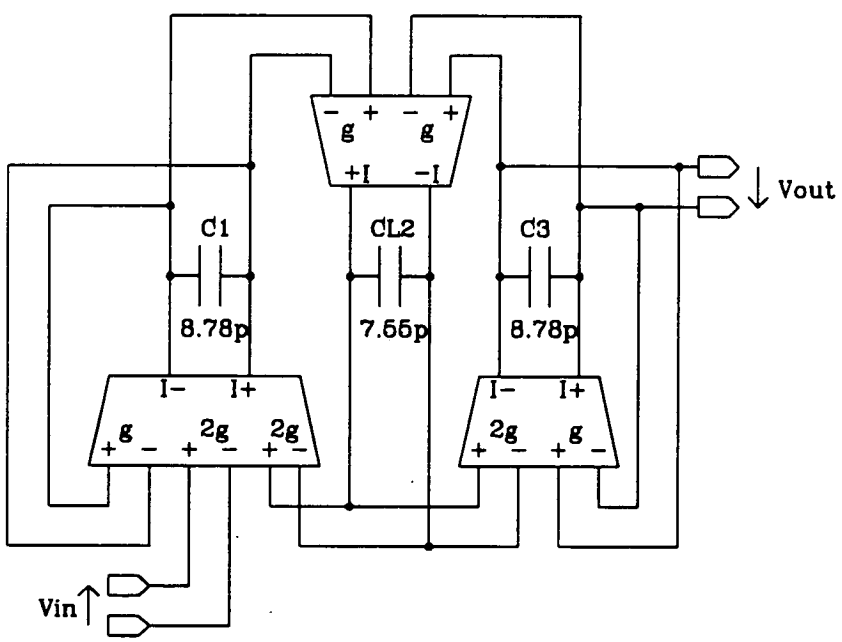


Figure 3.2-13 Third order all-pole lowpass transconductor ladder obtained by indirect simulation of prototype

The equivalence of directly and indirectly simulated filters exists as long as the latter method involves the independent simulation of each inductor current.

However this is not always possible. For example, if the passive prototype includes a closed loop of inductors, the simulation of each inductor current separately can lead to an unstable active circuit. This problem is illustrated later in this section.

Lowpass filters which require transmission zeros (such as elliptic filters) are implemented easily by direct or indirect simulation, as the capacitors associated with the zeros in the prototype map directly into capacitors in the active circuit. However two points require attention. Firstly, these capacitors are floating and so the value of each bottom plate parasitic must be subtracted from any grounded capacitor connected to the same node. This can be avoided by the use of low impedance transconductor inputs, as explained in chapters 5 and 6. Secondly, in a fully differential circuit two capacitors are required for each floating capacitor of the prototype. The values of these two should be increased by an extra factor of two since they are effectively in series for differential signals. As an example, a fifth order elliptic lowpass prototype and its active realisation scaled to a cutoff frequency of 1MHz are shown in figures 3.2-14 and 3.2-15. This circuit can be derived by both the component simulation and leapfrog methods. The result of a SPICE a.c. analysis of the transconductor ladder is shown in figure 3.2-16.

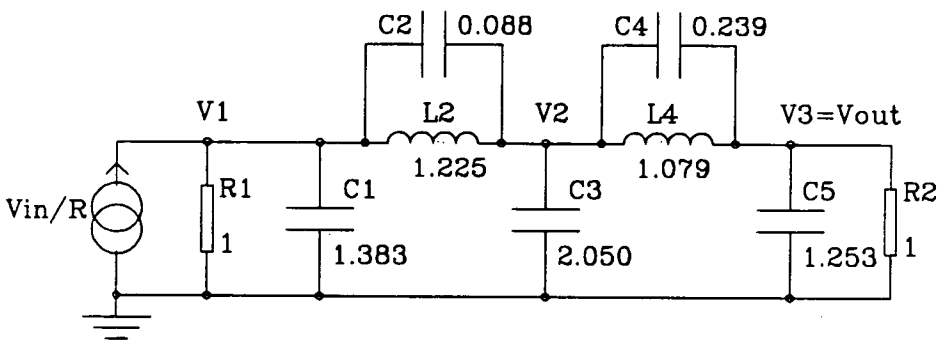


Figure 3.2-14 Prototype of fifth order elliptic lowpass ladder filter

Unfortunately the methods described above are only generally useful for a limited range of passive prototypes, such as lowpass filters of odd order and asymmetric all-pole bandpass filters. The fundamental reason for this is that the transconductor values in a filter do not represent a true degree of freedom. The resistive elements in SC and RC filters (switched capacitors and resistors respectively) can both be scaled freely, whereas it is undesirable to use more than one value of transconductance in a filter. This is because the transistors which determine the value of a particular transconductor can vary in size within only a small range without suffering from poor matching in one extreme or producing high parasitic capacitance and power consumption in the other. Moreover it is inconvenient for the designer to have to

produce a different set of ratioed transconductors for each new filter design.

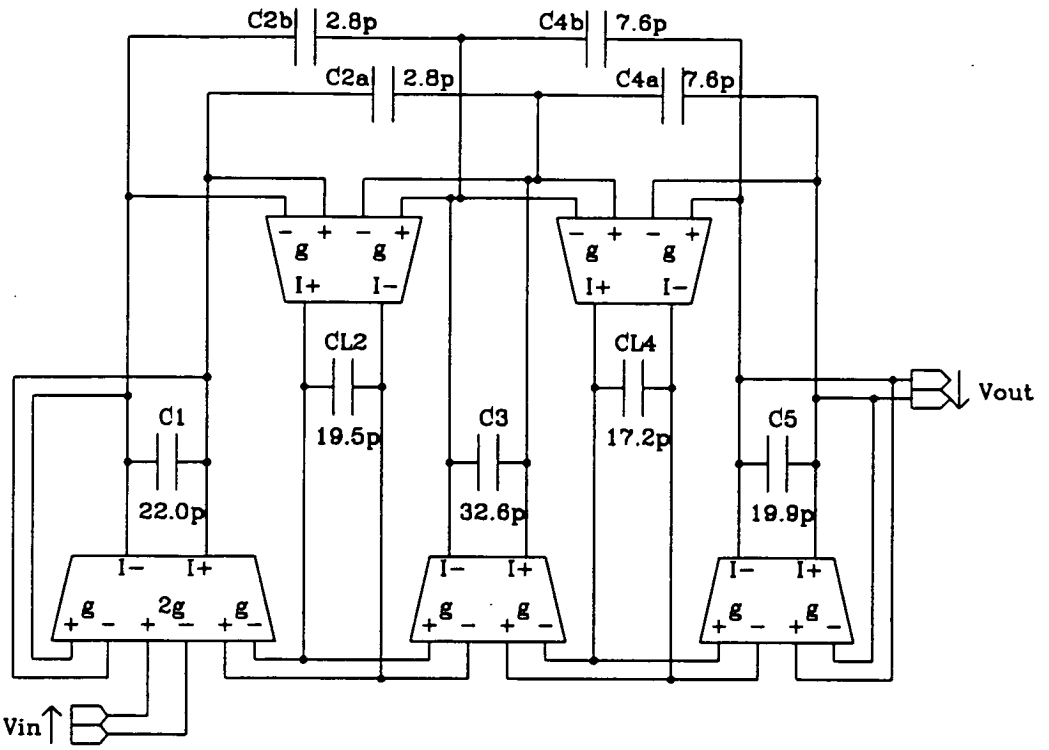


Figure 3.2-15 Fifth order lowpass lowpass elliptic transconductor ladder filter

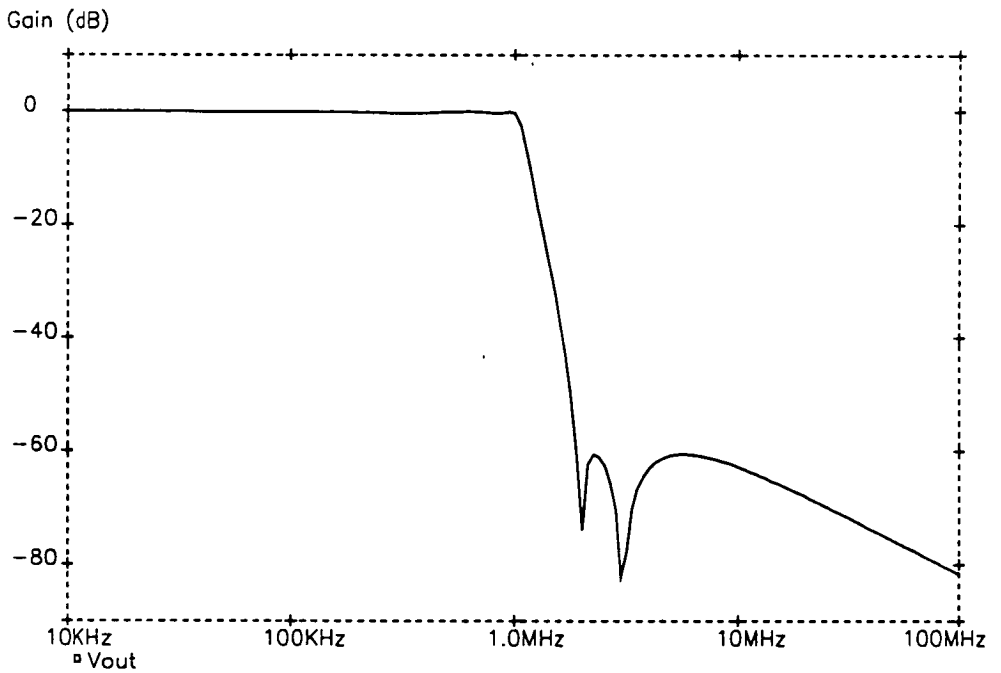


Figure 3.2-16

SPICE simulation of magnitude response of transconductor ladder (figure3.2-15)

Where ratioed transconductors are used, the ratios should be of low integer value so that they can be implemented by unit transconductors connected in parallel. This is the case in the design examples given above where 2:1 ratios are introduced in the course of nodal voltage scaling. In the remainder of this section, a number of examples are presented in which conventional design techniques lead to high or non-integer transconductor ratios.

First we consider the design of a sixth order Chebyshev symmetric bandpass filter. The prototype, normalised to a center frequency of 1rad/sec, is obtained from a third order lowpass ladder by applying the standard frequency tranformation, which we briefly summarise here [4,59]. A capacitor of value C in the lowpass ladder becomes a capacitor and an inductor in parallel in the bandpass ladder, of values C/bw and bw/C respectively where bw is the desired fractional bandwidth. An inductor of value L in the lowpass ladder becomes an inductor and capacitor in series in the bandpass ladder, with values L/bw and bw/L respectively. Figure 3.2-17 shows the ladder obtained by applying this transformation to a lowpass Chebyshev prototype with 0.1dB passband ripple (prototype C0315 in [59]), for a fractional bandwidth of 1.65%.

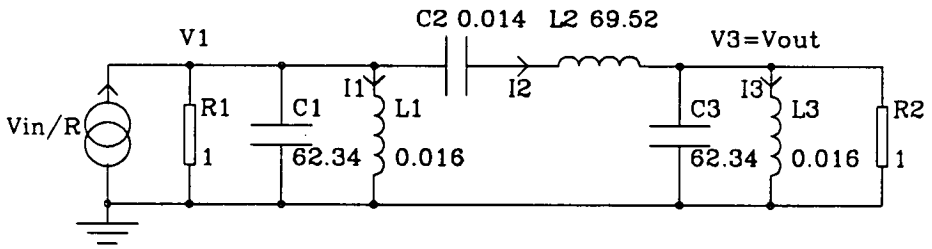


Figure 3.2-17 Sixth order symmetric Chebyshev bandpass prototype ladder

The operation of the passive ladder may be described by the following equations:

$$V_1 = \frac{1}{sC_1}[(V_{in}-V_1)/R-I_1-I_2]$$

$$I_1 = \frac{1}{sL_1}V_1$$

$$V_2 = \frac{-1}{sC_2}I_2$$

$$I_2 = \frac{1}{sL_2}[V_1+V_2-V_3]$$

$$V_3 = \frac{1}{sC_3}[I_2-I_3-V_3/R]$$

$$I_3 = \frac{1}{sL_3}V_3, \qquad (3.10a\text{-}f)$$

where V_i is the voltage across C_i and I_i is the current through L_i. Equations (3.10a-f) can be reexpressed:

$$V_1 = \frac{g}{sC_1}[V_{in}-V_1-V_{I1}-V_{I2}]$$

$$V_{I1} = \frac{g}{sC_{L1}}V_1$$

$$V_2 = \frac{-g}{sC_2}V_{I2}$$

$$V_{I2} = \frac{g}{sC_{L2}}[V_1+V_2-V_3]$$

$$V_3 = \frac{g}{sC_3}[V_{I2}-V_{I3}-V_3]$$

$$V_{I3} = \frac{g}{sC_{L3}}V_3, \qquad (3.11a\text{-}f)$$

where

$$V_{Ii} = I_iR \qquad (3.2\text{-}12)$$

and $$C_{Li} = \frac{L_i}{R^2} \qquad (3.2\text{-}13)$$

By simulating each of (3.11a-f) with a summing integrator the coupled biquad bandpass ladder shown in figure 3.2-18 is obtained. This circuit may be scaled easily to the desired impedance and centre frequency but the nodal voltage scaling is more problematic. Within each biquad the two integration capacitors differ in value by the factor $1/bw^2 \cong 61^2$. This causes severe gain peaking to occur on internal nodes, as is demonstrated by the SPICE a.c. simulation shown in figure 3.2-19.

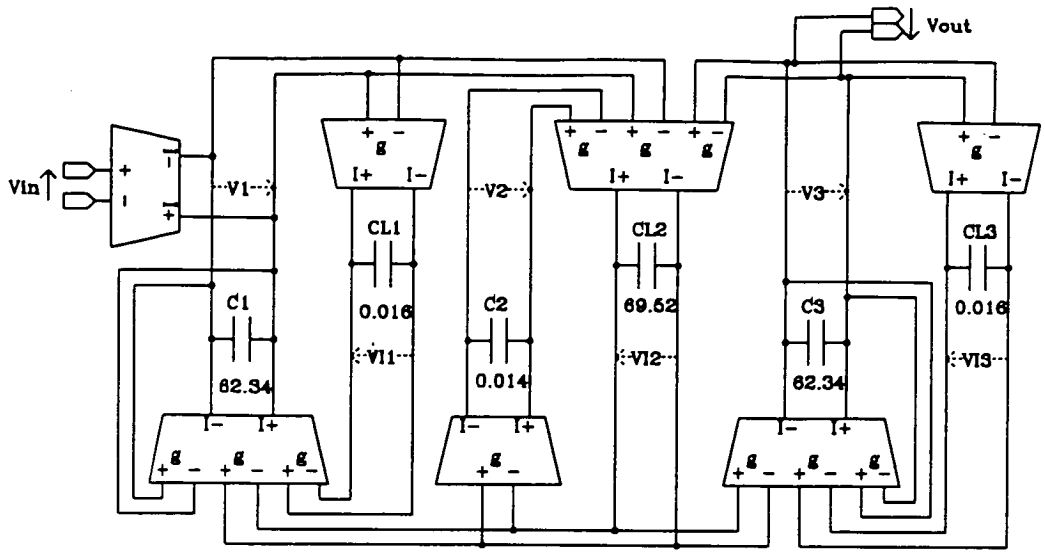


Figure 3.2-18 Unscaled bandpass transconductor ladder filter

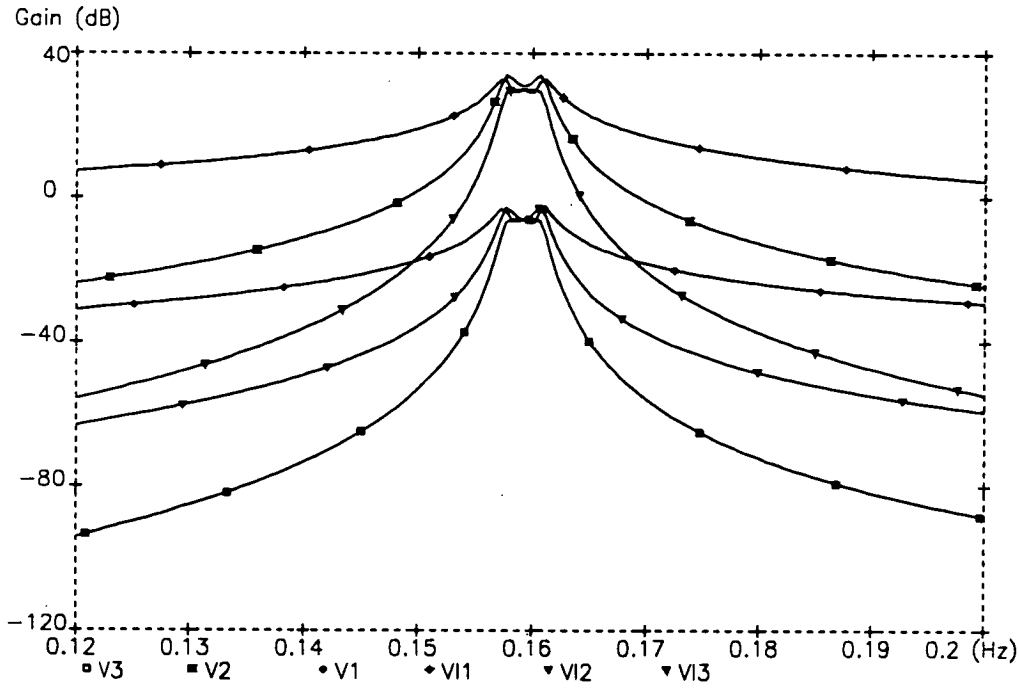


Figure 3.2-19 Nodal voltages of unscaled bandpass transconductor ladder filter

The nodal voltages of the filter may be scaled to more reasonable values by multiplying the large capacitors and dividing the smaller capacitors by the fractional bandwidth. To maintain the same transfer function, the transconductor inputs which are used for terminations and coupling between biquads must also be multiplied by bw, as shown in figure 3.2-20. The nodal voltages resulting from the magnitude scaling are illustrated in figure 3.2-21. Unfortunately the 61:1 transconductor ratios required by this design are very inconvenient in practice. On one hand, if a moderate

value of g is chosen then the g/61 transconductances may be very inaccurate due to the small transistor sizes. On the other hand, if a moderate value of g/61 is chosen, then the inputs of value g will have significant parasitic capacitance and require large bias currents. Such scaling can be tolerated for filters with moderately wide bandwidth [31] though it is not necesary to do so if the methods described in chapter 6 are applied. But it cannot be tolerated for highly selective filters, since the transconductance ratio generally takes a value close to the Q of the filter (Q being defined as the reciprocal of the fractional bandwidth). This is a serious problem because one of the main target applications for high frequency transconductor filters is in i.f. stages which are highly selective.

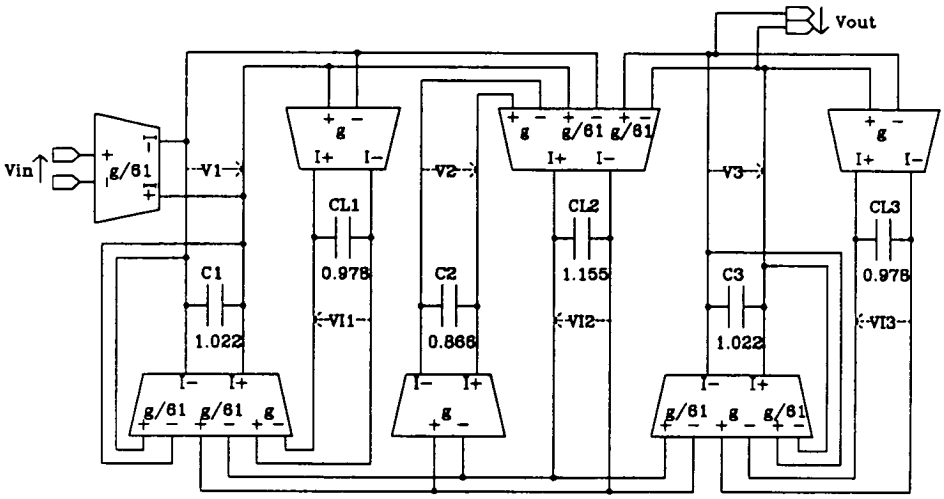


Figure 3.2-20 Bandpass transconductor ladder filter after voltage scaling

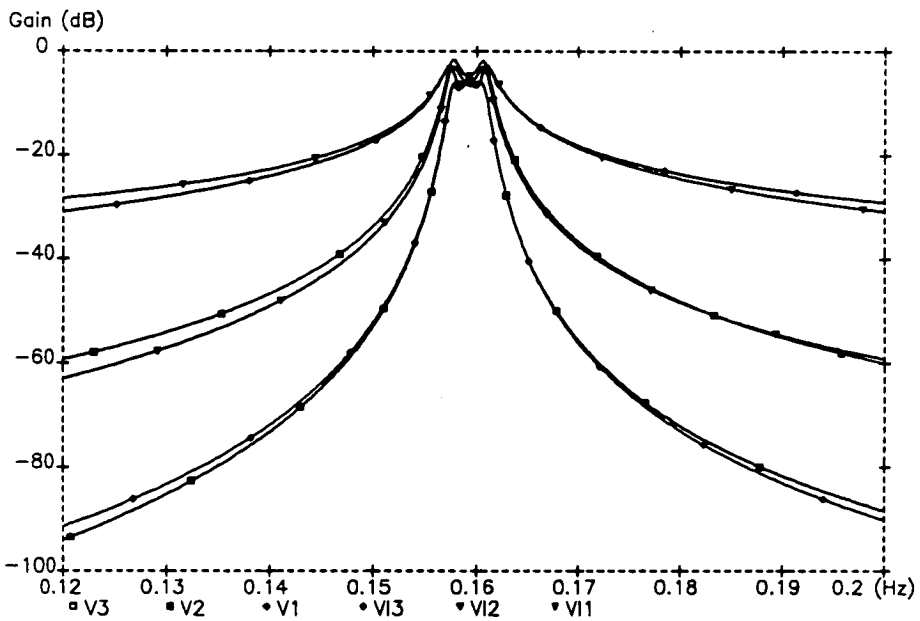


Figure 3.2-21 Nodal voltages of scaled bandpass transconductor ladder filter

The use of the smaller value of transconductance can be confined to the terminations of the filter by using an asymmetric prototype such as that shown in figure 3.2-22 [67]. This is beneficial because the termination resistors are the least sensitive components of the prototype and small errors in their effective value cause gain errors rather than distortion of the passband shape.

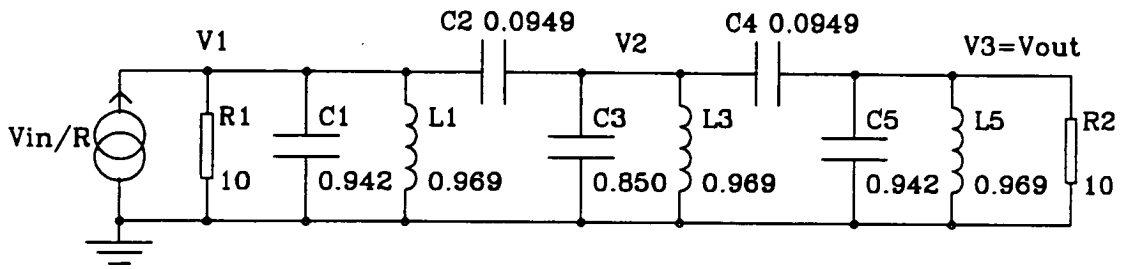


Figure 3.2-22 Sixth order asymmetric Chebyshev bandpass prototype ladder

The active circuit derived from this asymmetric prototype (which has 0.1dB ripple and 10% bandwidth) is shown in figure 3.2-23. The transfer functions of the symmetric and asymmetric filters are plotted together in figure 3.2-24 for comparison.

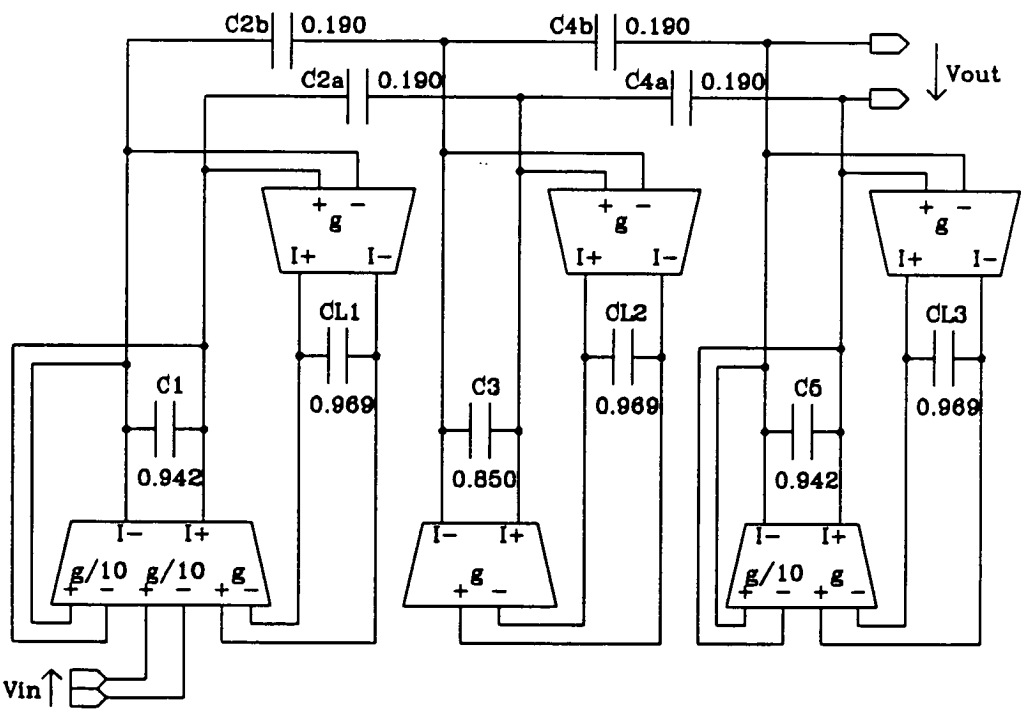


Figure 3.2-23 Asymmetric Chebyshev bandpass transconductor ladder

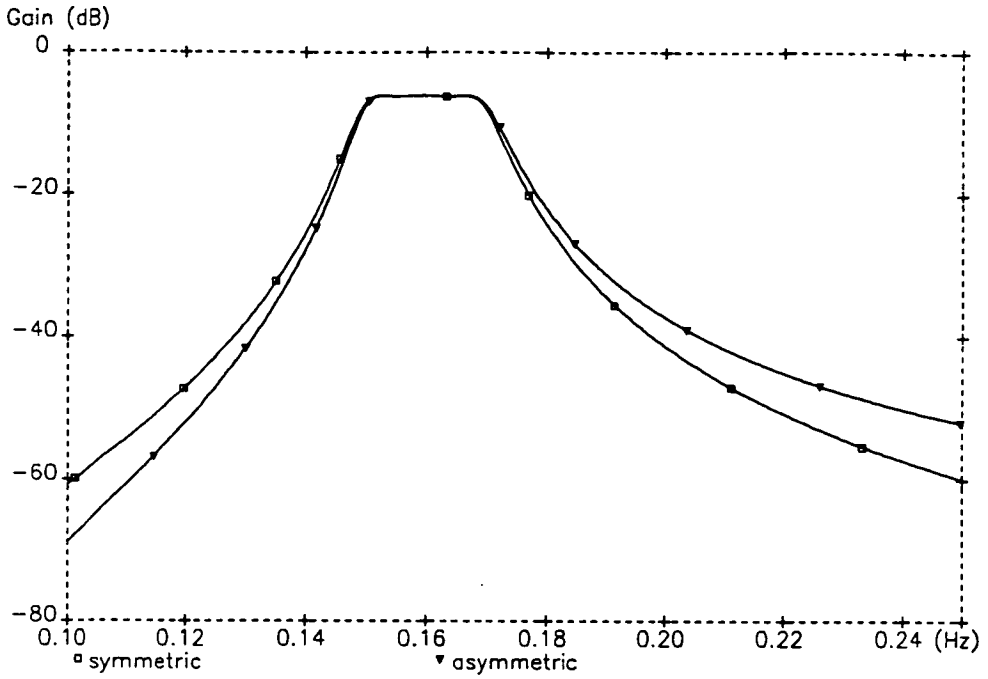


Figure 3.2-24 Magnitude responses of symmetric and asymmetric sixth order Chebyshev bandpass filters

Conventional design methods are found to be even more deficient when applied to a prototype containing closed loops of inductors, as occur in elliptic bandpass ladders. If each inductor current in such a loop is simulated individually, then the resulting active circuit is unstable. Instead, algebraic combinations of inductor currents must be simulated, which inevitably requires the use of non-integer transconductance ratios.

For example figure 3.2-25 shows the passive prototype of a sixth order elliptic bandpass filter.

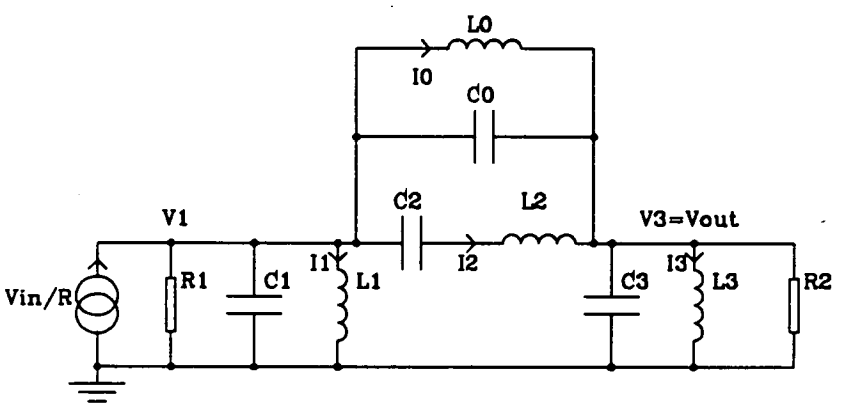


Figure 3.2-25 Passive prototype of a sixth order elliptic bandpass filter

If each inductor current were simulated individually, the design equations for the filter would be:

$$V_1 = \frac{g}{sC_1}[V_{in}-V_1-V_{I1}-V_{I0}-V_2]+\frac{C_0}{C_1}[V_3-V_1]$$

$$V_{I1} = \frac{g}{sC_{L1}}V_1$$

$$V_2 = \frac{-g}{sC_2}V_{I2}$$

$$V_{I2} = \frac{g}{sC_{L2}}[V_1+V_2-V_3]$$

$$V_{I0} = \frac{g}{sC_{L0}}[V_1-V_3]$$

$$V_3 = \frac{g}{sC_3}[V_{I2}+V_{I0}-V_{I3}-V_3]+\frac{C_0}{C_1}[V_1-V_3]$$

$$V_{I3} = \frac{g}{sC_{L3}}V_3 \qquad (3.2\text{-}14a\text{-}g)$$

where the symbols are as defined in the previous examples. In practice each of equations (3.2-14a-g) would be simulated by an integrator which has its own input offset voltage. For the filter to be stable the quiescent input to each integrator must cancel that integrator's offset voltage. Therefore, (3.2-14b) and (3.2-14g) indicate that the quiescent values of V_1 and V_3 must equal the input offset voltages of the integrators which generate V_{I1} and V_{I3} respectively. However (3.2-14e) shows that the combination (V_1-V_3) must also equal the offset of the V_{I0} integrator. Since the offsets are to an extent random, the two voltages V_1 and V_3 cannot simultaneously meet the three constraints imposed upon them and so this active filter would be unstable. This problem can be avoided by not simulating each of the inductor currents individually [19]. Instead new variables are introduced:

$$I_a = I_0+I_1 \qquad (3.2\text{-}15)$$

$$I_b = I_3-I_0 \qquad (3.2\text{-}16)$$

$$V_a = V_{I0}+V_{I1} \qquad (3.2\text{-}17)$$

$$V_b = V_{I3}-V_{I0}. \qquad (3.2\text{-}18)$$

These are used to derive an alternative set of design equations by algebraic combination of (3.2-14a-g):

$$V_1 = \frac{g}{sC_1}[V_{in}-V_1-V_a-V_{I2}]+\frac{C_0}{C_1}[V_3-V_1]$$

$$V_a = \frac{g}{sC_{10}}[V_1-aV_3]$$

$$V_2 = \frac{g}{sC_2}V_{I2}$$

$$V_{I2} = \frac{g}{sC_{L2}}[V_3-V_2-V_1]$$

$$V_b = \frac{g}{sC_{30}}[V_3-bV_1]$$

$$V_3 = \frac{g}{sC_3}[V_{I2}-V_b-V_3]+\frac{C_0}{C_1}[V_1-V_3] \qquad (3.2\text{-}19a\text{-}f)$$

where

$$C_{i0} = \frac{C_{Li}C_{L0}}{C_{Li}+C_{L0}} = g^2\frac{L_iL_0}{L_i+L_0} \qquad (3.2\text{-}20)$$

$$a = \frac{C_{L1}}{C_{L1}+C_{L0}} = \frac{L_1}{L_1+L_0} \qquad (3.2\text{-}21)$$

$$b = \frac{C_{L3}}{C_{L3}+C_{L0}} = \frac{L_3}{L_3+L_0}. \qquad (3.2\text{-}22)$$

It is clear from (3.2-21) and (3.2-22) that a and b will generally have non-integer values, and that the design equations (3.2-19a-f) will have summing coefficients in non-integer ratios. Therefore whilst this method has been used successfully for SC filters, it will be unsuitable for transconductor filters.

A simpler example of a passive prototype which would require inconvenient transconductor values is the fourth order Chebyshev ladder shown in figure 3.2-26, which has termination resistors of unequal value (as does any even order Chebyshev or elliptic low pass ladder).

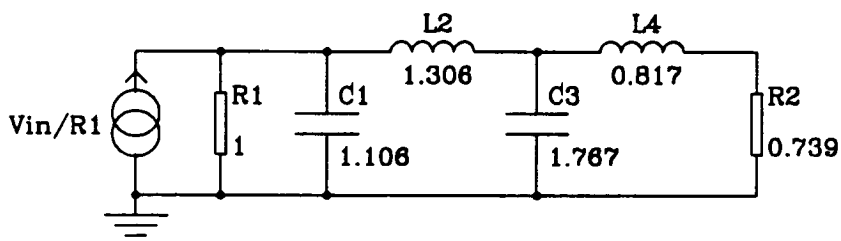


Figure 3.2-26 Fourth order Chebyshev lowpass prototype ladder

In this section we have described the direct and indirect simulation methods conventionally used to derive transconductor ladder filters, and their limitations have been demonstrated. In chapters 5 and 6 new methods are introduced which enable the design of a much greater range of transconductor ladders.

3.3 Frequency control

The simplest form of control loop [20] is shown in figure 3.3-1. In this scheme the transconductance is forced to take the value equal to a fraction of the conductance of an off chip precision reference resistor. An on chip potential divider applies a voltage aV_{ref} to the input of the transconductor so that its output current is $(aV_{ref})gm$. This current passes through the reference resistor of value R_{ref}, and the voltage across it, $(aV_{ref})gmR_{ref}$, is applied to the negative input of the opamp. The high gain of the negative feedback loop formed by the opamp and the transconductor forces the two inputs of the opamp to be at the same potential (or in practice separated by the input offset voltage of the opamp). Thus the control voltage V_c takes a value such that :

$$(aV_{ref})gmR_{ref} = V_{ref} \tag{3.3-1}$$

Therefore

$$gm = \frac{1}{aR_{ref}} \tag{3.3-2}$$

The compensation capacitor is required to keep the phase margin of the feedback loop high enough to prevent oscillation.

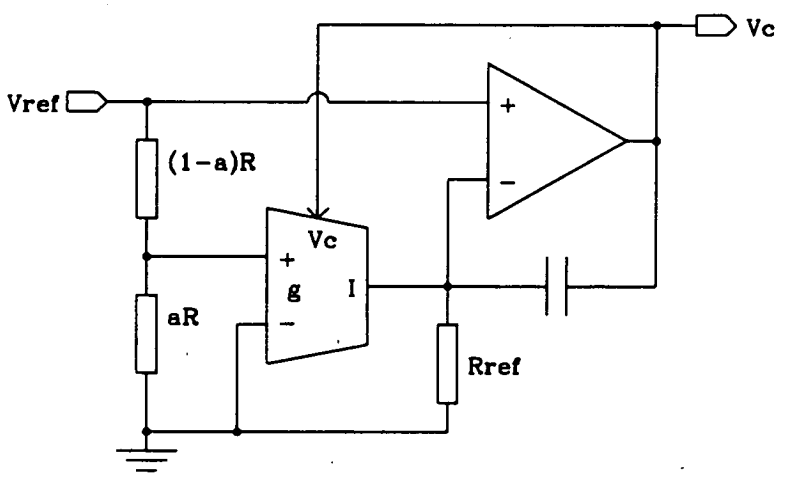


Figure 3.3-1 Reference resistor control loop

The reference resistor control loop has the disadvantage of requiring a discrete component of very precise value and low temperature coefficient. A more fundamental drawback is that it does not take account of the wide tolerance in the

values of the *capacitors* in the filter. A fully automatic tuning scheme should set the values of filter time constants (of the form C/gm) rather than transconductance values alone. In fact the control loop of figure 3.3-1 can be modified to do this by replacing the reference resistor by a switched capacitor simulated resistor [32] as shown in figure 3.3-2.

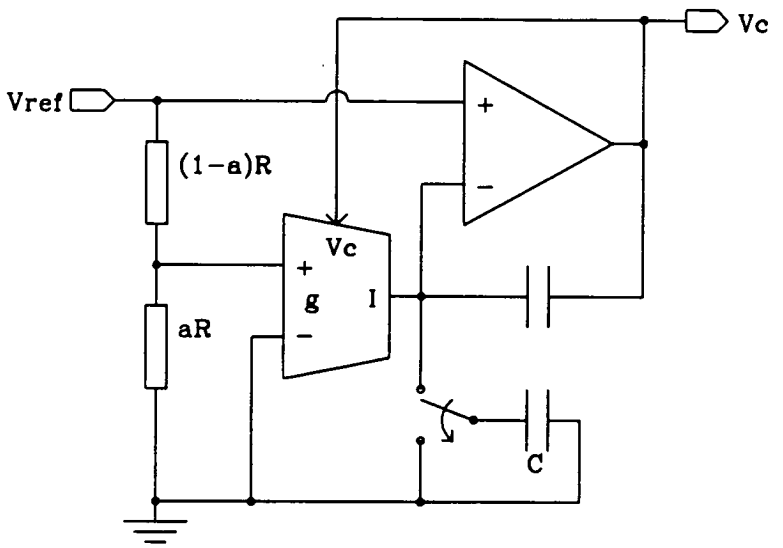


Figure 3.3-2 Switched capacitor control loop

The analysis of this circuit proceeds as before but with R_{ref} replaced by the value of the switched capacitor's effective resistance which is $1/f_SC$, where f_S is the frequency of the switching clock and C is the value of the capacitor. Then we find from equation (3.3-2) that:

$$gm = \frac{f_S C}{a} \tag{3.3-3}$$

which can be rearranged to show the value of the time constant:

$$\tau = \frac{C}{gm} = \frac{a}{f_S} \tag{3.3-4}$$

Thus the time constant in the control loop is determined by a clock frequency and a resistor ratio. Since the capacitors and transconductors in the filter are ratio matched to those in the control loop, the time constants in the filter are also set and an accurate filter response is obtained.

A decoupling capacitor (usually external) is necessary to prevent components

at the clock frequency and its harmonics from appearing on the control voltage line. Any non d.c. term in V_C will modulate the values of all the transconductors to cause distortion and aliassing.

A more common method for setting the time constants of a transconductor filter is to use a phase lock loop [68] as a control loop . The PLL can be built around either a voltage controlled oscillator (VCO) [30,43] or a voltage controlled filter (VCF) [24,27]. In both cases, the voltage controlled element contains transconductor integrators whose time constant is forced by the loop to track the frequency of an externally generated clock signal. As in the simpler loops described above, the control voltage within the PLL is passed to the transconductors of the filter so that the filter time constants track those of the control loop.

Figure 3.3-3 shows a PLL which consists of a VCO, a phase comparator and a low pass filter (LPF). We first consider the case in which the reference signal is a sinusoid, the VCO is a harmonic oscillator and the phase detector is a linear multiplier. The VCO can be formed from two integrators connected back to back with no damping components. The amplitude of the oscillations must be restricted to prevent the integrators saturating to the supply voltages. For the limiter it is possible to use either a non-linear device such as a diode-connected MOSFET [43] or a linear amplitude dependent impedance [30]. Alternatively the amplitude can be set by a Q control loop [54], as described in the following section.

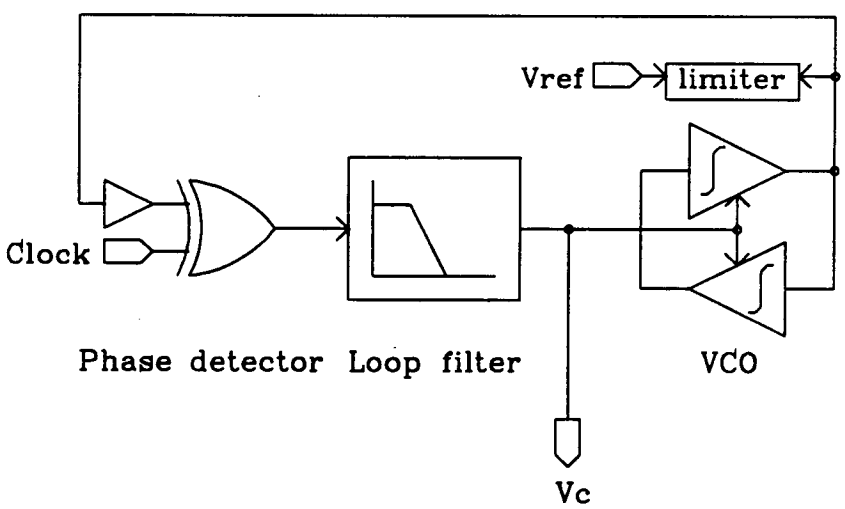


Figure 3.3-3 PLL frequency control lock with a harmonic VCO

If the circular frequency of the reference signal is ω and the VCO output differs in phase and frequency from the reference by ϕ and $\Delta\omega$, then the output of the phase detector is

$$V_{PD} = K\cos(\omega t)\cos(\phi+\omega t+\Delta\omega t)$$
$$= 0.5K[\cos(\phi+\Delta\omega t)\{1+\cos(2\omega t)\}-\sin(\phi+\Delta\omega t)\sin(2\omega t)] \qquad (3.3\text{-}5)$$

where K is the product of the multiplier gain and the amplitudes of the two inputs signals. If the bandwidth of the LPF, ω_0, satisfies the condition

$$\Delta\omega < \omega_0 << \omega \qquad (3.3\text{-}6)$$

then the output of the LPF, which equals the control voltage, is

$$V_C = 0.5K\cos(\phi+\Delta\omega t). \qquad (3.3\text{-}7)$$

When the PLL is in a steady state, the value of V_C should be static. From (3.3-7) it is seen that this condition can only be satisfied if $\Delta\omega=0$, i.e. if the VCO frequency is equal to that of the reference signal. If the V_C does have to change, say to compensate for a change in temperature, then this will be effected by a change in the value of ϕ.

We have analysed a PLL based on a linear VCO, however other systems are possible. In chapter 7 a control loop is described in which the reference signal is a square wave, the VCO is non-harmonic, requiring only one integrator, and the phase detector is an XOR gate.

Figure 3.3-4 shows a PLL control loop employing a VCF [27]. The VCF is a second order highpass section, which ideally has a phase shift of 90^o at its cutoff frequency. The phase detector is implemented as a multiplier so its output will have no d.c. component when the two inputs differ in phase by 90^o. If the cutoff frequency of the VCF does not equal the reference frequency, then the phase detector inputs will not differ in phase by 90^o and a d.c. error will be generated at the output of the detector. This error signal is multiplied by the d.c. amplifier, whose output is used as the control voltage. The feedback of the loop is negative so that the control voltage forces the VCF response to be such that its input and output differ in phase by 90^o, which ideally implies that the cutoff of the VCF equals the reference frequency.

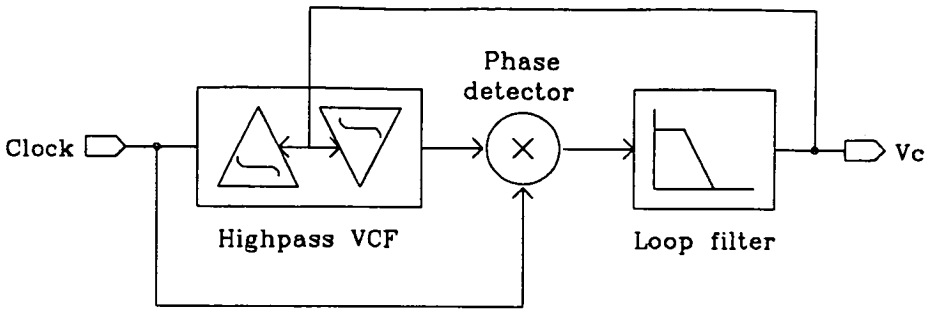


Figure 3.3-4 PLL control loop using a VCF

The disadvantage of the VCF control loop is that it relies on an *absolute* measurement of phase, in contrast to the VCO loop which relies on a measurement of the first derivative of phase (i.e. frequency). This makes the VCF loop succeptible to any d.c. errors in the phase measurement, which may arise from several sources such as the input offset voltage of the phase detetector and parasitic poles in the VCF.

Further discussion of frequency control is given in chapter 7 where the control loop used in the experimental circuits is described.

3.4 Phase control

As was stated in section 3.1, the master-slave system may be extended by additional "masters" to compensate for distortion of the filter response by transconductor phase errors (appendix A). We refer to these masters as Q (or phase) control loops.

In a ladder filter a single Q control loop may be used, generating a second control voltage (in addition to the ubiquituous frequency control voltage) which is distributed to each integrator. In a cascaded biquad filter a separate Q control loop may be included for each biquad [16,18], which adjusts the value of one transconductor responsible for the Q of that biquad. As in the case of frequency control, a Q control loop can be based on either a VCF or a VCO and it is possible to combine the frequency and Q control loops using a single VCF or VCO in a vector lock loop (VLL).

The basis of any Q control loop is an amplitude locked loop (ALL). (Care should be taken to avoid confusion with terminology: a *phase* lock loop is used to control *frequency*, and an *amplitude* lock loop is used to control *phase*.) The relationship between amplitude and Q control can be illustrated with respect to the biquad shown in figure 3.4-1.

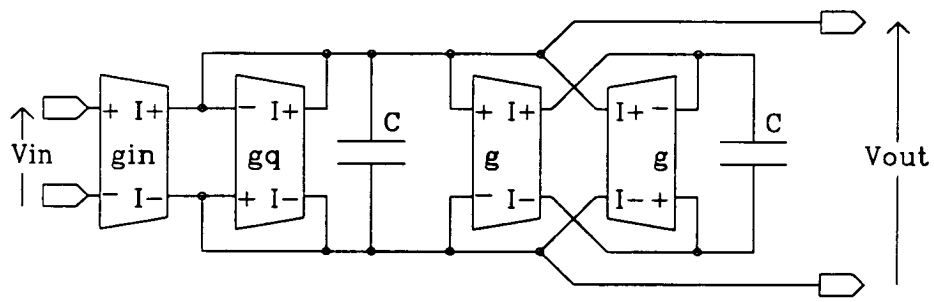


Figure 3.4-1 Transconductor bandpass biquad

This biquad has the transfer function:

$$H(s) = \frac{\frac{sg_{in}}{Q}}{s^2 + \frac{sg_q}{C} + \left(\frac{g}{C}\right)^2} \qquad (3.4\text{-}1)$$

The general transfer function for a bandpass biquad can be written

$$H(s) = A\frac{\frac{s\omega_o}{Q}}{s^2+\frac{s\omega_o}{Q}+\omega_o{}^2}, \qquad (3.4\text{-}2)$$

where A is the gain at the centre circular frequency ω_0, and Q is the quality factor. Equating coefficients with (3.4-1) gives

$$A = \frac{g_{in}}{g_q} \qquad (3.4\text{-}5)$$

$$Q = \frac{g}{g_q} \qquad (3.4\text{-}6)$$

$$\omega_o = \frac{g}{C}. \qquad (3.4\text{-}7)$$

We now assume that the parasitic poles of each transconductor can be approximated by a single pole at $-1/\tau$, which is much higher than the signal frequencies of interest. Then each of g_{in}, g_q and g should be multiplied by the factor $(1+s\tau)^{-1}$ which can be approximated to $(1-s\tau)$ by the binomial theorem with the assumption that the magnitude of $s\tau$ is much less than one at the frequencies of interest. If this frequency dependence is included in (3.4-1) and only the dominant terms retained, the transfer function becomes

$$H(s) = \frac{\frac{sg_{in}}{C}}{s^2+\frac{sg_q}{C}(1-2Q\omega_o\tau)+\left[\frac{g}{C}\right]2} \qquad (3.4\text{-}8)$$

Again equating coefficients with (3.4-2) we find

$$A = \frac{(1-2Q\omega_o\tau)g_{in}}{g_q} \qquad (3.4\text{-}9)$$

$$Q = \frac{(1-2Q\omega_o\tau)g}{g_q} \qquad (3.4\text{-}10)$$

$$\omega_o = \frac{g}{C}. \qquad (3.4\text{-}11)$$

This shows that to first order the dependences of the gain and quality factor of the biquad upon excess phase, $\omega_0\tau$, are identical. Therefore it is reasonable to expect that an ALL may be able to correct simultaneously for errors in gain and quality factor.

A block diagram of a VCF based ALL is shown in figure 3.4-2. The VCF can be a second order section, such as the bandpass biquad described above. The Q control voltage can adjust directly the value of one of the transconductors, such as g_q in the bandpass biquad. Alternatively if the transconductors used have variable phase compensation [18], such as that described in section 5.3, the Q control voltage will be routed to each of them. The input to the VCF is a reference signal of fixed amplitude. The output of the VCF and the reference signal multiplied by the desired filter gain A are both full wave rectified or squared, so that they are effectively amplitude demodulated. The difference between the two demodulated signals is integrated (or low pass filtered) with a very long time constant and the output of the integrator is used as the Q control voltage. The feedback is negative and the d.c. gain of the integrator is very large, so the difference between the amplitudes of the two integrator inputs is forced to a very low value and hence the gain of the of the VCF is made to equal A.

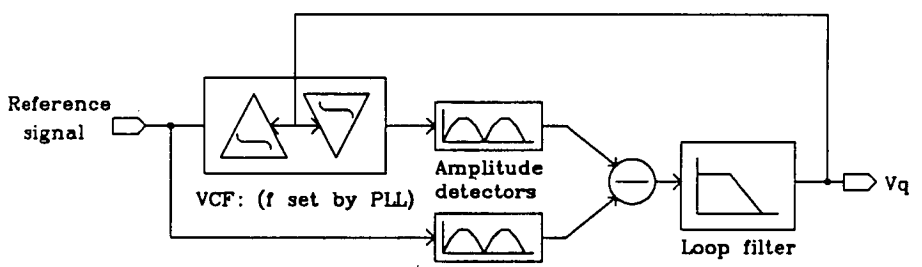


Figure 3.4-2 Amplitude lock loop using a voltage controlled filter

An ALL based on a harmonic VCO [54] is shown in Figure 3.4-3. The harmonic oscillator is composed of two transconductor integrators with variable phase control. The principal upon which this circuit is based is that the amplitude of oscillation will remain constant only if the phase shift (ϕ) in each integrator is exactly -90^o. Any phase lead ($|\phi|<90^o$) will effectively damp the oscillation and any phase lag ($|\phi|>90^o$) will cause the amplitude to increase. The amplitude demodulators and the integrator, which act as an error amplifier, adjust the phase control voltage such that the amplitude oscillation converges to that of the reference signal. In fact it is not critical that the two amplitudes equal each other, merely that the oscillation amplitude

remains constant.

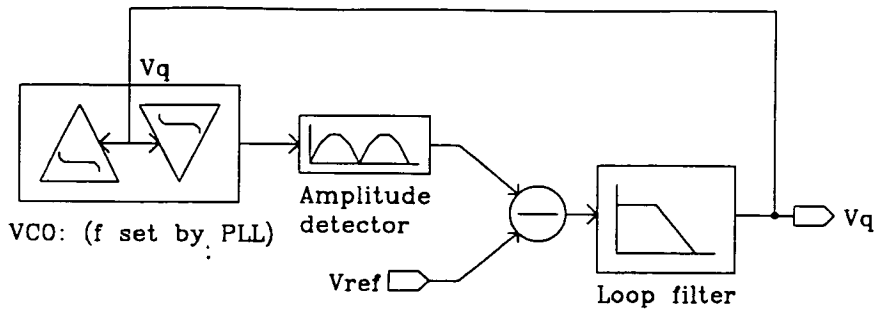


Figure 3.4-3 Amplitude lock loop using a voltage controlled oscillator

As in the case of the frequency control loop, the VCO based system appears to be preferable because it holds constant a parameter's derivative rather than its absolute value, thereby remaining immune to system offsets.

CHAPTER 4
THE GROUNDED QUAD TRANSCONDUCTANCE CELL

4.1 Introduction

In this chapter we introduce an original MOS configuration [63] which is capable of linear voltage to current conversion and demonstrate its application in a simple transconductor.

The new MOS transconductance cell is illustrated in figure 4-1.1. It consists of two input devices operating in saturation mode, each of which is degenerated with respect to the negative supply by the channel conductance of another transistor operating in triode mode. The input voltage is applied differentially to the gates of the saturation mode devices. For a fully differential circuit the output current is taken as half of the difference between the two currents produced. The transconductance of the quad is controlled by the voltage Vc applied to the gates of the triode mode devices, which adjusts their channel conductance. An expression for the d.c. transfer function is derived in section 4.2.

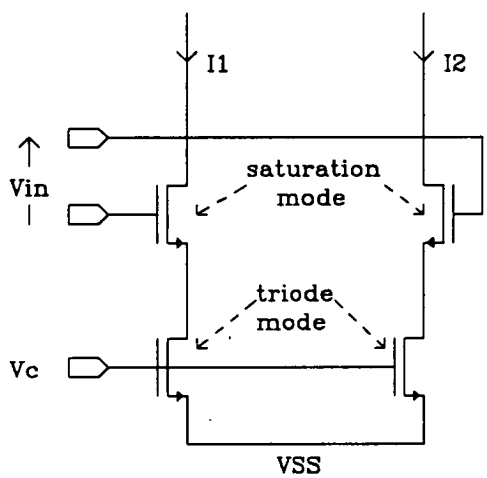


Figure 4.1-1 N-type grounded quad transconductance cell

A single-stage grounded quad transconductor is presented in section 4.3. In the next chapter a set of folded cascode transconductors is described which use the grounded quad cell as their input stage. Both the single stage and the folded cascode transconductors are used in the experimental filters (chapter 7).

4.2 Analysis

To develop a useful transfer function for the grounded quad cell we make the simplifying assumptions that, for a particular control voltage, the channel resistance of each triode mode device has a value R independent of the input signal, and that the body effect can be neglected. The grounded quad can then be represented by the equivalent circuit shown in figure 4.2-1.

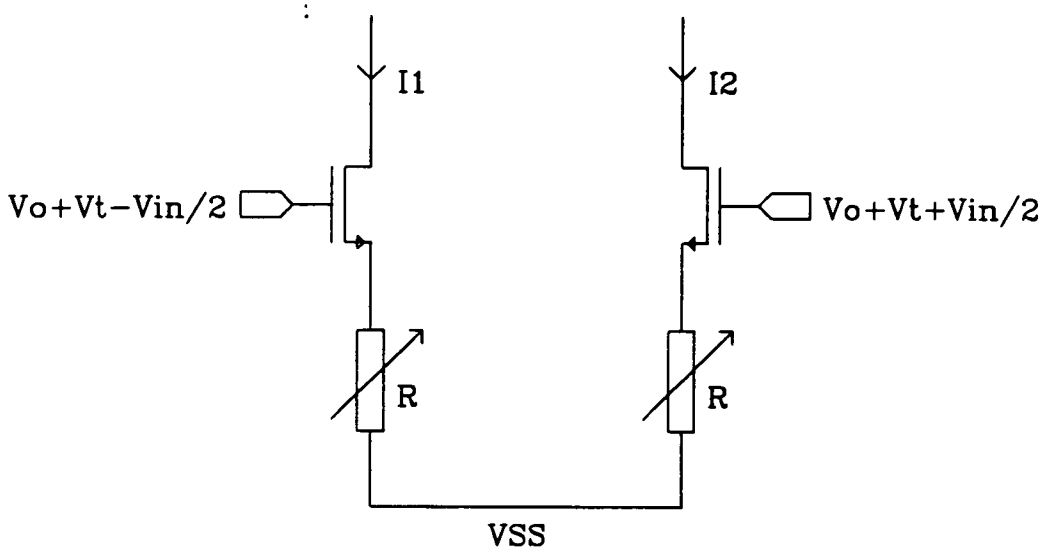


Figure 4.2-1 Grounded quad equivalent circuit

First we find the current in one side of the quad. Into the standard equation (B-3)

$$I = 0.5\beta(V_{gs}-V_t)^2 \tag{4.2-1}$$

for the current in a saturated MOSFET we make the substitution

$$V_{gs}-V_t = \frac{V_{in}}{2}+V_o-IR, \tag{4.2-2}$$

where V_{in} is the differential input voltage, V_o is the difference between the signal ground with respect to the negative supply rail and the threshold voltage, and IR is the voltage across the channel of the triode mode device. Then the resulting quadratic equation is solved to obtain

$$I = \frac{1+\beta RV_o+\beta R\frac{V_{in}}{2}-\sqrt{1+2\beta RV_o+\beta RV_{in}}}{\beta R^2} \tag{4.2-3}$$

The current in the other side of the cell is given by an equation identical to (4.2-3) but with $V_{in}/2$ replaced by $-V_{in}/2$. We take the mean of the difference between these two currents to obtain the output current

$$I_{out} = \frac{V_{in}}{2R} - \frac{c}{2\beta R^2}\left[\sqrt{1+\beta R\frac{V_{in}}{c^2}} - \sqrt{1-\beta R\frac{V_{in}}{c^2}}\right] \qquad (4.2\text{-}4)$$

where

$$c = \sqrt{1+2\beta R V_O}. \qquad (4.2\text{-}5)$$

Equation (4.2-5) is simplified by expanding the square roots and retaining terms up to the third harmonic:

$$I_{out} = \frac{V_{in}}{2R}(1-c^{-1}) - \frac{R\beta^2}{16c^5}V_{in}^3 \qquad (4.2\text{-}6)$$

It is clear from (4.2-6) that the most linear behaviour is obtained when the transconductance of the saturation devices is much greater than the channel conductance of the triode devices. The product βR and the term c then tend to large values, such that the third harmonic is deemphasised and the overall transconductance tends to 1/2R. This limit, which is intuitively obvious, corresponds to the differential input voltage simply being levelshifted onto the drains of the triode devices. Unfortunately the limit cannot be exploited too far, as making the saturation devices wide burdens the transconductor with a large input capacitance and making the triode devices too small is detrimental to matching. However even when all the devices in the quad cell are of similar dimensions the third harmonic of (4.2-6) is very small, as is confirmed by simulation results in this chapter and experimental results in chapter 7.

Since the transconductance is a function of the common mode level of the input signal, care should be taken with power supply decoupling and with the common mode feedback of the circuit from which the input is taken (usually another identical transconductor).

4.3 A single-stage grounded quad transconductor

In addition to its linearity, the grounded quad cell is attractive for its simplicity and the absence of saturation mode devices in series makes it particularly suitable for use in low voltage processes. As an example figure 4.3-1 shows a complete single-stage grounded quad transconductor designed for use in a 1μ CMOS process the nominal supply for which is 5V. A p-type quad is used, loaded with a pair of n channel devices. The bias for the active load is provided by a common mode feedback error amplifier which holds the mean of the voltages at the output nodes close to the midrail voltage AGND. Figure 4.3-2 shows the double input version of this transconductor in which two quads share one CMFB and active load circuit.

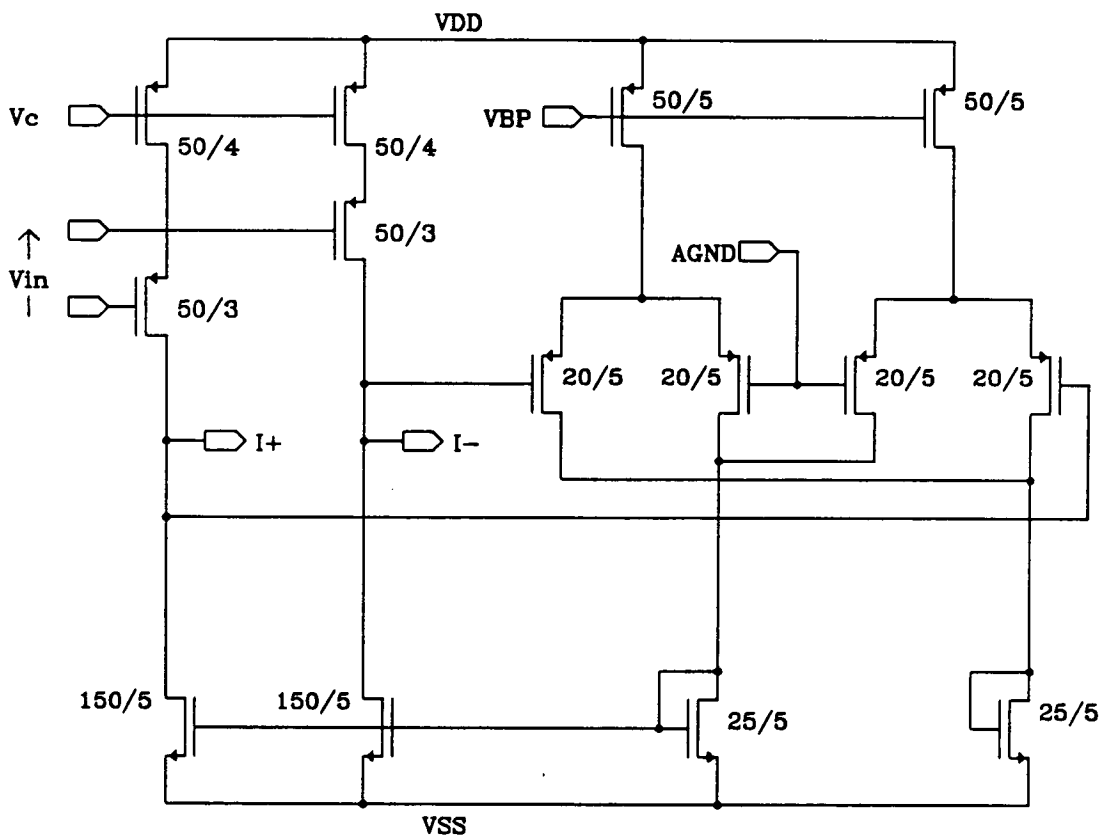


Figure 4.3-1

Schematic of fully differential single-stage grounded quad transconductor

A filter using a double input version of this transconductor (figure 4.3-2) is included on one of the test chips described in chapter 7. Measured results for this filter (LPF2) are given in section 7.3. Experimental results are not available for the transconductor alone, however some SPICE simulation results are given in this section for the single input transconductor.

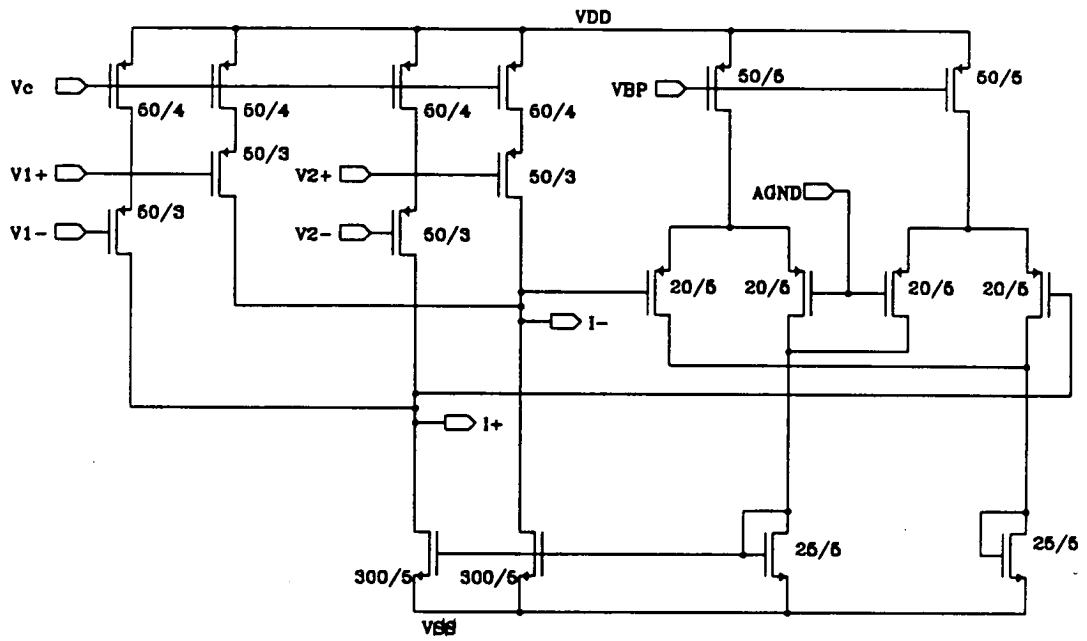


Figure 4.3-2 Double input grounded quad transconductor

Figure 4.3-3 shows the result of an a.c. simulation of the single input transconductor configured as an integrator with 1MHz unity gain frequency. The two curves show the magnitude and phase of the differential voltage transfer function. The phase shift at the unity gain frequency is -89.75°.

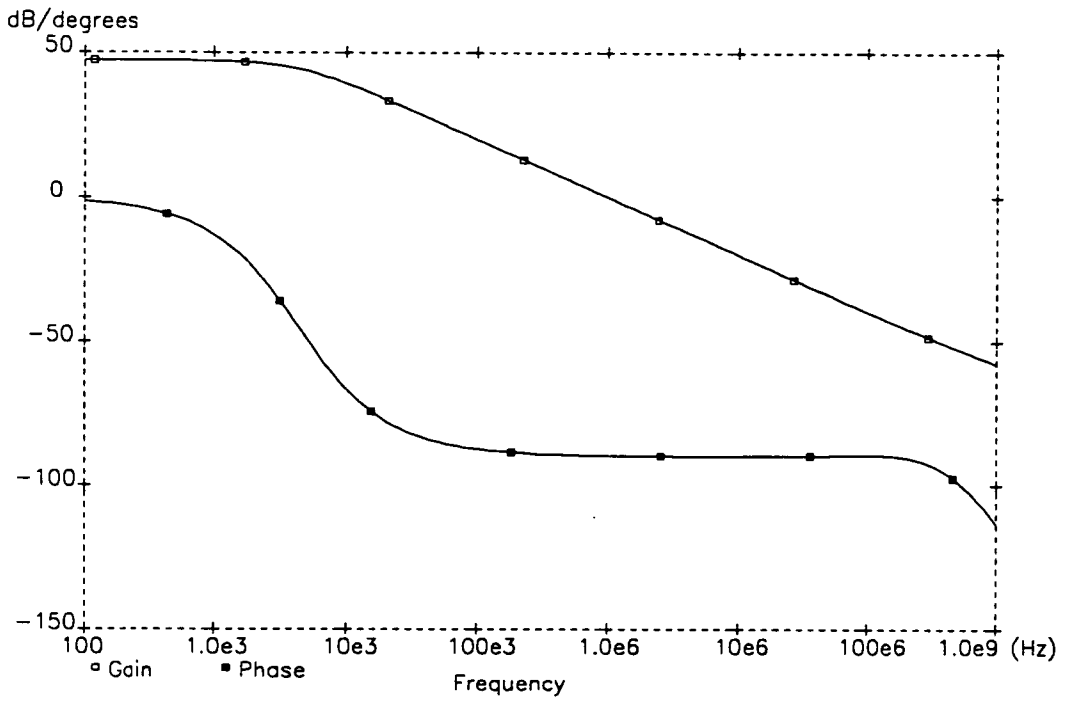


Figure 4.3-3

a.c. simulation of grounded quad transconductor with 30.4pF differential load

The next simulation shows the common mode transfer function of the transconductor, again configured as a 1MHz integrator. The d.c. value of the common mode rejection, 5.8dB, is equal to the common mode transconductance of the grounded quad divided by that of the common mode feedback circuit. It is particularly important that a filter using this transconductor should have negligible common mode signals since the transconductance of a grounded quad is influenced by the input common mode voltage. Any modulation of the transconductance will cause harmonic distortion.

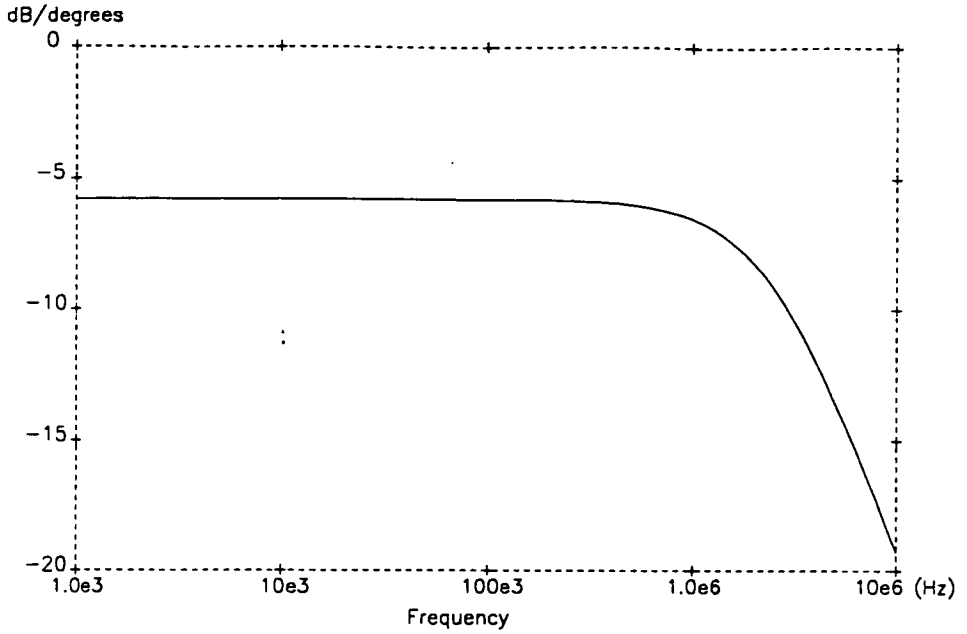


Figure 4.3-4 a.c. simulation of common mode rejection

The remaining two plots illustrate the d.c. linearity of the transconductor. The first shows the output current as a function of input voltage, with a small signal transconductance of 100μS. The second shows the percentage error in output current as a function of input voltage. It should be stressed that the linearity depends strongly on the relative aspect ratios of the triode and saturation mode transistors in the grounded quad and also the value of the control voltage. Further work is required to determine the optimum values for these.

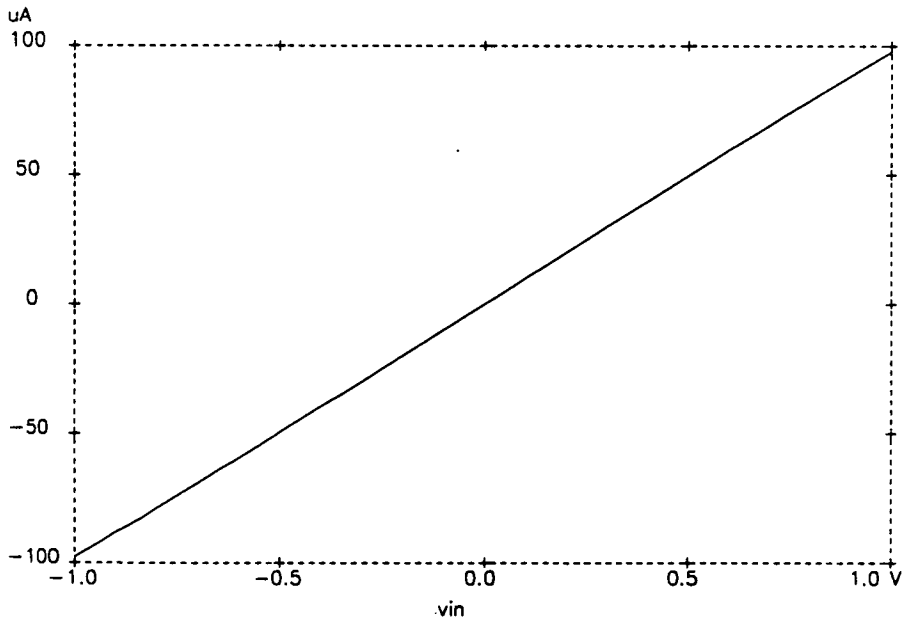


Figure 4.3-5 d.c. simulation of transconductor output current versus input voltage

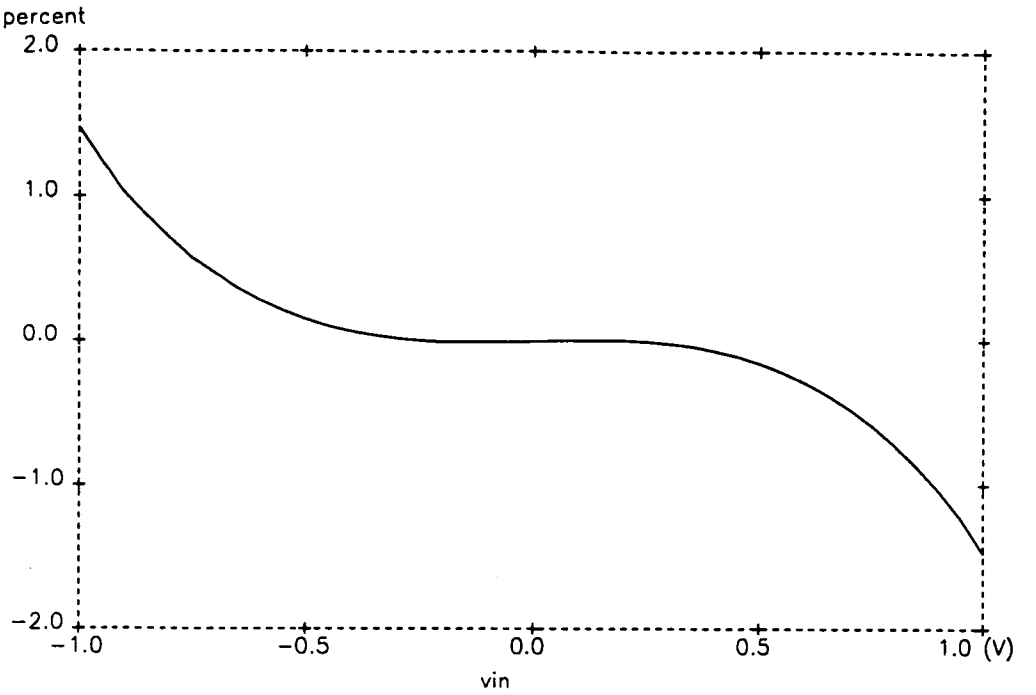


Figure 4.3-6 Error of transconductor output current as a function of input voltage

CHAPTER 5
FOLDED CASCODE TRANSCONDUCTORS

5.1 Introduction

Many of the transconductor circuits presented in chapters 2 and 4 are single-stage, in the sense that the output current is taken from the drains of the same transistors to which the input voltage is applied [24,28]. The motivation for using such simple circuits is to maximise the frequencies of any parasitic poles and hence reduce excess phase effects. In this respect single-stage transconductors are successful, and they have been used in lowpass filters with cutoff frequencies up to 4MHz [30] without Q-control.

Unfortunately single-stage CMOS transconductors are not so suitable for bandpass filters or lowpass filters with very flat passbands, due to their relatively low values of output impedance [57]. Bandpass filters are more sensitive than lowpass filters to the voltage gain of the transconductor, which equals the product of the transconductance and the output impedance. This sensitivity increases with the selectivity of the filter.

Another drawback of a single-stage CMOS transconductor is that its voltage swing in the region of the unity gain frequency is limited to approximately one threshold voltage (i.e. < 1V) as signals greater than this will turn the input devices into triode mode, causing severe distortion. This point of course applies equally to lowpass filters.

Both problems described above can be solved by the use of folded cascode (FC) transconductors [63]. Such circuits are linearised versions of the folded cascode operational transconductance amplifiers (OTA's) used routinely in switched capacitor circuits [23] and occasionally used in continuous time filters [71]. The linearisation can be achieved by the same techniques used for single-stage transconductors but without the accompanying dynamic range limitations since the output is no longer taken from the drains of the input devices. The cascode structure provides a very

high output impedance.

In the following section the folded cascode structure is analysed and examples of FC transconductors are given. In section 5.3 we show how low impedance current summing inputs can be included in a FC transconductor circuit by the addition of only a few extra components. This is a very important development as it allows the design of ladder filters requiring no transconductance ratios, by the methods introduced in chapter 6. A further modification to the FC transconductor circuit provides the facility for variable phase error compensation, for those applications in which automatic Q control is required. This is discussed in section 5.4.

5.2 Analysis and examples

A generalised fully differential folded cascode transconductor is shown in figure 5.2-1. The voltage to current (V-I) input stage can be a p-type version of one of the transconductive cells described in chapters 2 and 4, such as a degenerated long tail pair or a grounded quad cell. We let g_{in} denote its transconductance. V_{BN}, V_{CN}, V_{CP} and V_{BP} are bias voltages, at least one of which would in practice be supplied by a common mode feedback (CMFB) circuit.

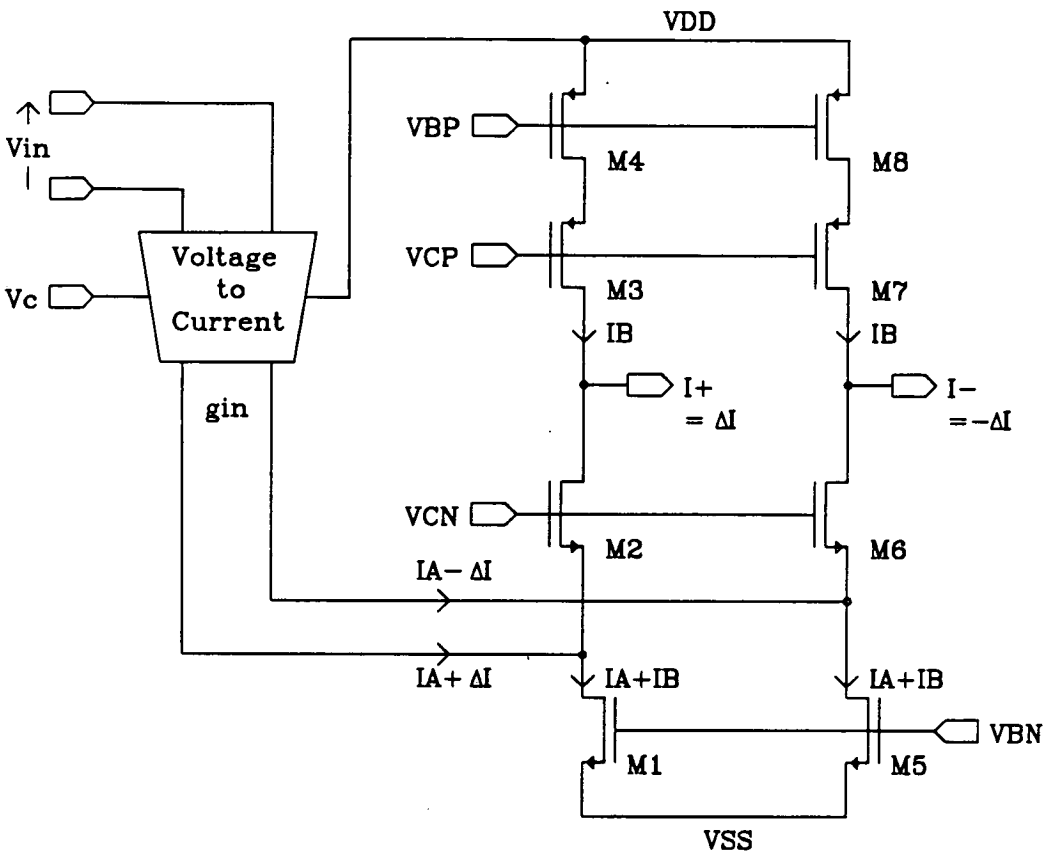


Figure 5.2-1 General fully differential folded cascode transconductor

First we examine one side of figure 5.2-1 to see how the output current is produced. The current from the V-I input stage consists of a quiescent component I_A plus a signal component ΔI, equal to $g_{in}V_{in}$. The p-type MOSFETs M_3 and M_4 form a cascode source of current I_B. The bias on M_1 is designed such that its channel current is (I_A+I_B), therefore in order that charge be conserved in the cascode chain the output current must equal ΔI.

To obtain expressions for the output impedance, transconductance and voltage gain, we analyse the small signal equivalent circuit, figure 5.2-2, of one side of the

transconductor. Each transistor M_i is modelled as the parallel combination of its transconductance g_i and its drain source conductance g_{dsi}, and the input stage is modelled by a transconductance g_{in} and an output impedance z_{VI}. The g_i term is of course omitted for those transistors with fixed gate-source voltage.

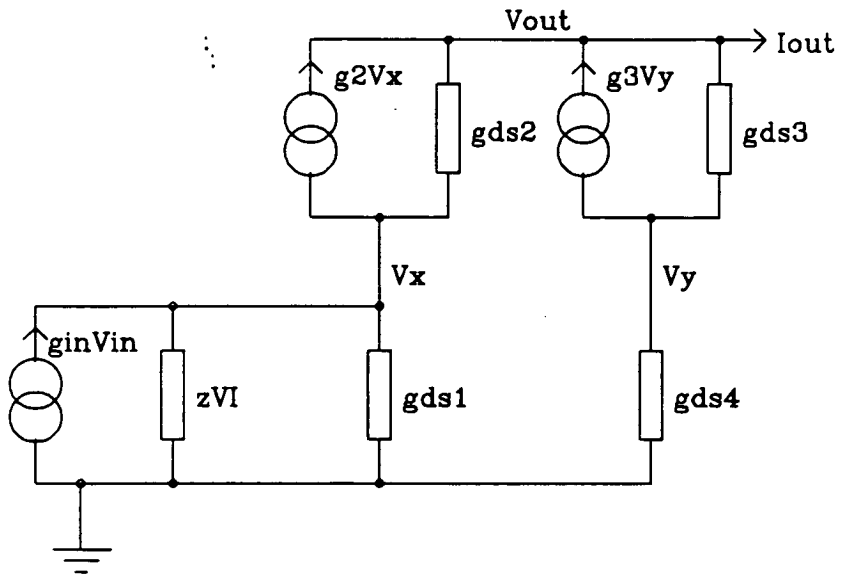


Figure 5.2-2 Small signal equivalent circuit of one side of figure 5.2-1

Applying Kirchhoff's current law and some algebraic manipulation to the equivalent circuit yields the following expression for the output current:

$$I_{out} = \left[1 - \frac{z_{VI}^{-1}+g_{ds1}}{g_2+z_{VI}^{-1}+g_{ds1}+g_{ds2}}\right] g_{in}V_{in}$$

$$- \left[\frac{g_{ds2}(z_{VI}^{-1}+g_{ds1})}{g_2+z_{VI}^{-1}+g_{ds1}+g_{ds2}} + \frac{g_{ds3}g_{ds4}}{g_3+g_{ds3}+g_{ds4}}\right] V_{out} \qquad (5.2\text{-}1)$$

This equation is greatly simplified by making the assumptions that $g_{in} >> g_{dsj}$ and $g_i >> g_{dsj}$, for any i and j:

$$I_{out} = \left[1 - \frac{z_{VI}^{-1}+g_{ds1}}{g_2}\right] g_{in}V_{in} - \left[\frac{z_{VI}^{-1}+g_{ds1}}{\alpha_2} + \frac{g_{ds4}}{\alpha_3}\right] V_{out} \qquad (5.2\text{-}2)$$

where

$$\alpha_i = \frac{g_i}{g_{dsi}} \tag{5.2-3}$$

is the gain of transistor M_i. The transconductance, gm, and output impedance, Z_{out}, of the FC circuit are found by differentiating (5.2-2):

$$gm = \frac{\delta I_{out}}{\delta V_{in}} = \left[1 - \frac{z_{VI}^{-1} + g_{ds1}}{g_2}\right] g_{in} \cong \left[1 - \frac{2}{\alpha}\right] g_{in} \tag{5.2-4}$$

$$Z_{out} = \frac{-\delta V_{out}}{\delta I_{out}} = \left[\frac{z_{VI}^{-1} + g_{ds1}}{\alpha_2} + \frac{g_{ds4}}{\alpha_3}\right]^{-1} \cong \frac{\alpha}{g_{ds}} \tag{5.2-5}$$

where α and g_{ds} are typical values of MOSFET gain and output conductance. A crude expression for the voltage gain, A_V, can then be found:

$$A_V = gmZ_{out} \cong \alpha \frac{g_{in}}{g_{ds}}. \tag{5.2-6}$$

In section 2.2 the output impedance and gain of a single stage transconductor were shown to be of the order of g_{ds}^{-1} and g_{in}/g_{ds} respectively. Equations (5.2-5) and (5.2-6) indicate that the corresponding quantities for the FC transconductor are greater by a factor approximately equal to the gain of a MOSFET. The value of α is in the region of 30 to 40dB for standard size devices. Hence we can expect the voltage gain of a typical FC transconductor to be at least 70dB.

Equation (5.2-4) indicates that the transconductance of the FC circuit is very slightly less than that of its input stage, due to the finite output impedances of M_1 and the input stage itself.

The only internal signal carrying node of the conventional folded cascode structure is that connecting the input stage, the drain of M_1 and the source of M_2, so we can assume that the high frequency behaviour will be dominated by the parasitic capacitance, C_p, at this point. To find an expression for the pole associated with C_p we notice that the conductance of this capacitor is in parallel with g_{ds1}. Equation (5.2-1) is then modified to:

$$I_{out} = \left[\frac{(g_2+g_{ds2})g_{in}}{g_2+z_{VI}^{-1}+g_{ds1}+g_{ds2}+sC_p}\right]V_{in}$$

$$- \left[\frac{g_{ds2}(z_{VI}^{-1}+g_{ds1}+sC_p)}{g_2+z_{VI}^{-1}+g_{ds1}+g_{ds2}+sC_p} + \frac{g_{ds3}g_{ds4}}{g_3+g_{ds3}+g_{ds4}}\right]V_{out} \qquad (5.2\text{-}7)$$

and the transconductance is

$$g_m = \left[\frac{g_2+g_{ds2}}{g_2+z_{VI}^{-1}+g_{ds1}+g_{ds2}+sC_p}\right]g_{in}$$

$$\cong \frac{g_{in}}{1-\frac{s}{p}} \qquad (5.2\text{-}8)$$

where the value of the pole is

$$p \cong \frac{-g_2}{C_p}. \qquad (5.2\text{-}9)$$

The excess phase of the FC transconductor will be determined by this pole and those associated with the input stage.

A folded cascode transconductor based on the grounded quad cell is shown in figure 5.2-3. The nominal transconductance is 100μS for V_C = 2.28V. As in the case of the single-stage circuit a p-type input is used since this requires larger devices (for a given transconductance) which improves matching between transconductors. Common mode stability is provided by an error amplifier, figure 5.2-4, formed from two differential pairs. This adjusts the bias voltage V_{BN} such that the mean of the two output voltages remains close to midrail. The transconductance of these pairs needs to be kept low so that they do not saturate for large differential output voltage swings.

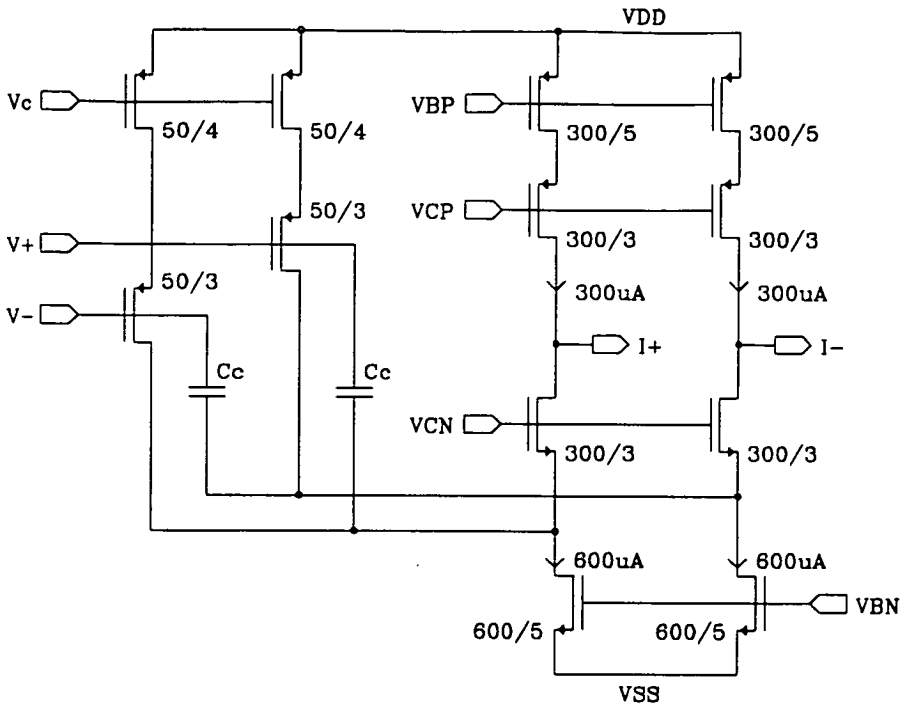


Figure 5.2-3 Folded cascode transconductor with grounded quad input stage

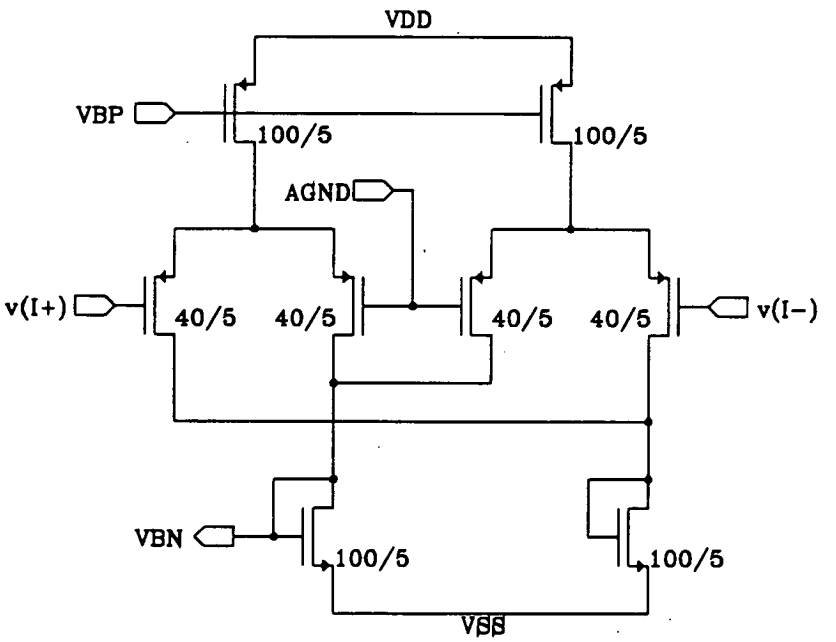


Figure 5.2-4 CMFB circuit for use with folded cascode transconductors

The results of a SPICE AC analysis are shown in figure 5.2-5. A 79.58pF load was connected between each of the outputs and ground, giving an effective differential load of 39.79pF and a unity gain frequency of 400kHz. The phase at the unity gain frequency is -90.01^{o} which is close enough to the ideal value (-90^{o}) to give very little distortion in a filter passband. This good phase performance is

achieved by the high output impedance and by the inclusion of the compensation capacitors (each marked Cc). These introduce a high frequency zero (at circular frequency 2gm/Cc) into the transfer function of the transconductor to provide first order cancellation of the effects of parasitic poles. The optimum value of Cc (150fF) was found by iteration of the AC simulation.

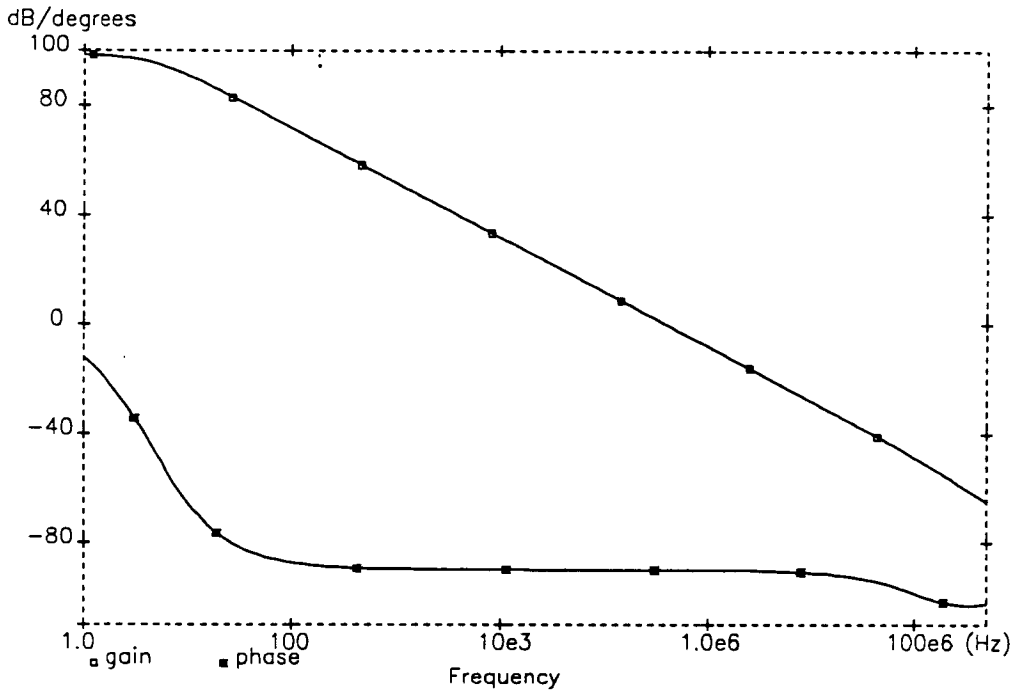


Figure 5.2-5 a.c. simulation of folded cascode transconductor (figure 5.3-3)

Figure 5.2-6 shows the output current as a function of input voltage and figure 5.2-7 represents the output error expressed as a percentage of full scale current. For input voltages in the range +/-1V, the output current is within 0.5% of the ideal value (100μA at 1V). The full scale current is equal to the quiescent current (300μA) in the cascode devices, therefore the output current modulation in this range is 33%. The accuracy of this FC transconductor falls off gently with increasing input voltage in contrast to the abrupt current limiting effect seen in single-stage transconductors.

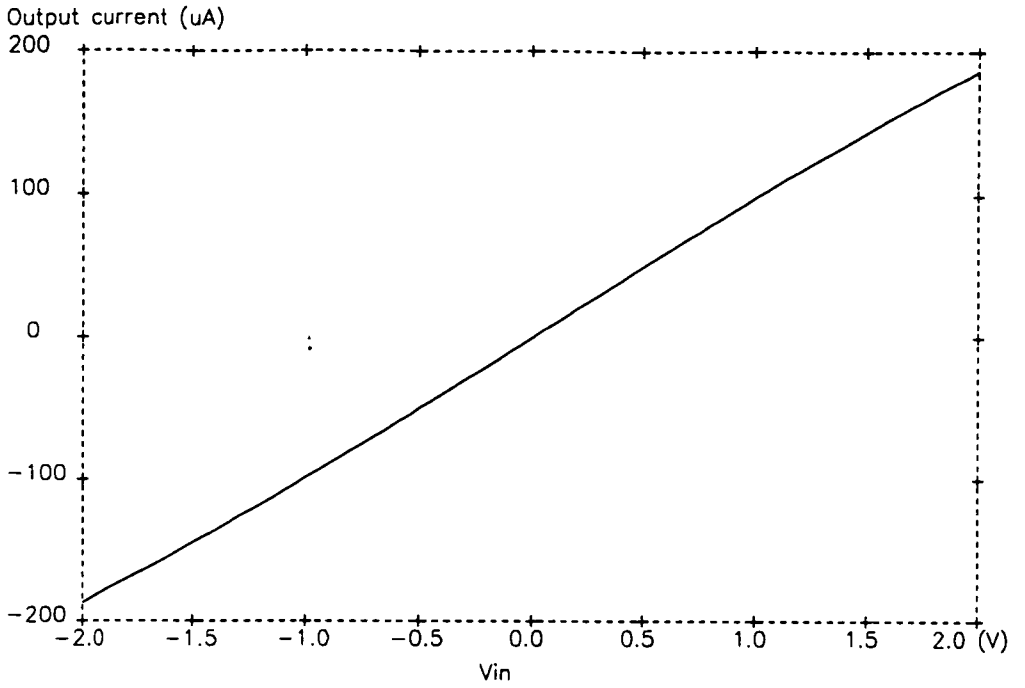


Figure 5.2-6

Simulated d.c. output current of folded cascode transconductor (figure 5.2-3)

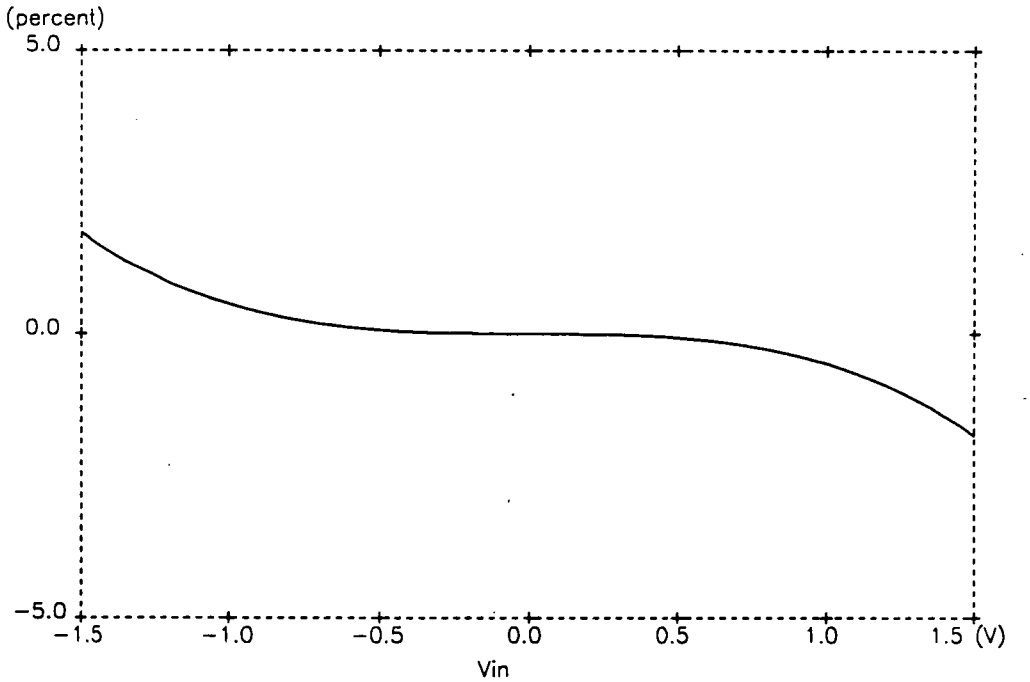


Figure 5.2-7 Error in output current of folded cascode transconductor (figure 5.2-3) with respect to full scale current

Figure 5.2-8 shows the simulated total harmonic distortion of the transconductor as a function of root mean square (rms) input voltage amplitude. These data were

obtained by processing the result of a SPICE transient analysis using the .FOUR card [22]. The transconductor was loaded with a 10kΩ resistor to give unity voltage gain.

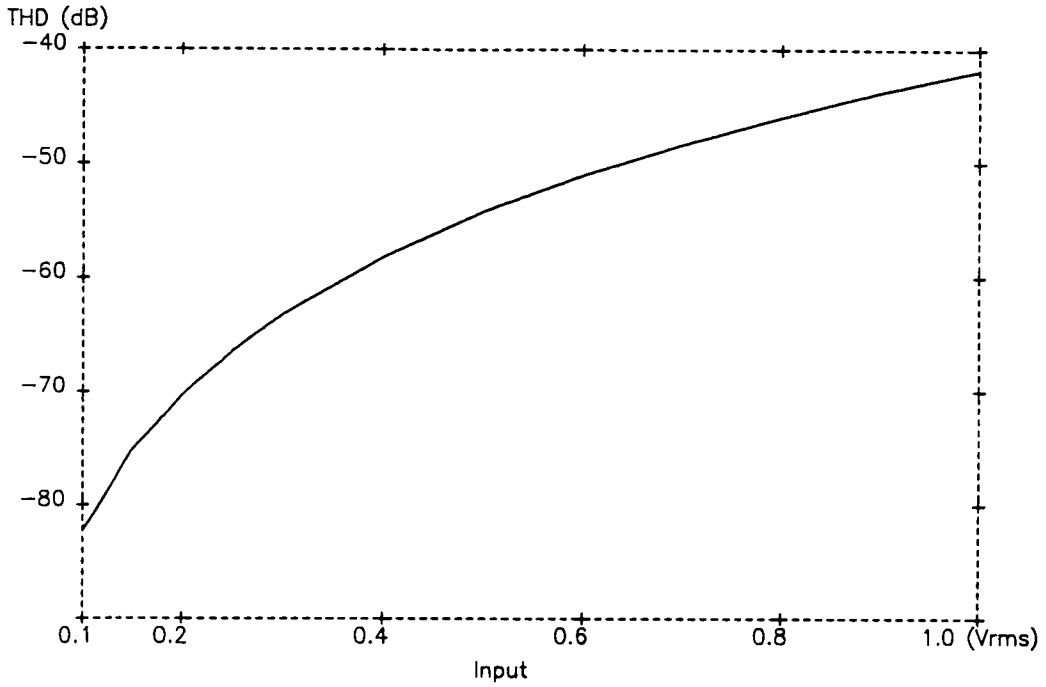


Figure 5.2-8

Simulated THD of folded cascode transconductor as a function of rms input voltage

The circuit used to generate the bias voltages for the grounded quad FC transconductor is shown in figure 5.2-9. The reference current is set by half of a grounded quad with its input connected to the signal common mode level (AGND) and with the same control voltage as supplied to the transconductor. In order to give maximum dynamic range, the cascode bias voltages (V_{CN} and V_{CP}) are designed to be as close as possible to the supply voltages whilst keeping the outer bias transistors of the transconductor in saturation mode [19].

Figures 5.2-10 and 5.2-11 give two examples of multi-input transconductors. The first, called FCGMD, has two inputs of transconductance 100μS. The second, FCGMQ10, has inputs of transconductance 100μS and 10μS. These transconductors are used in filters LPF1 and BPF1 respectively, which are described in chapter 7. The relative magnitudes of the inputs are set by ratioing the aspect ratios of the transistors in each grounded quad. It is also necessary to adjust the sizes of the n-type current sink transistors in each transconductor so that the correct bias currents are set in the cascode chains. Figure 5.2-12 is a photomicrograph of the double input transconductor, as used in experimental filter LPF1 (chapter 7).

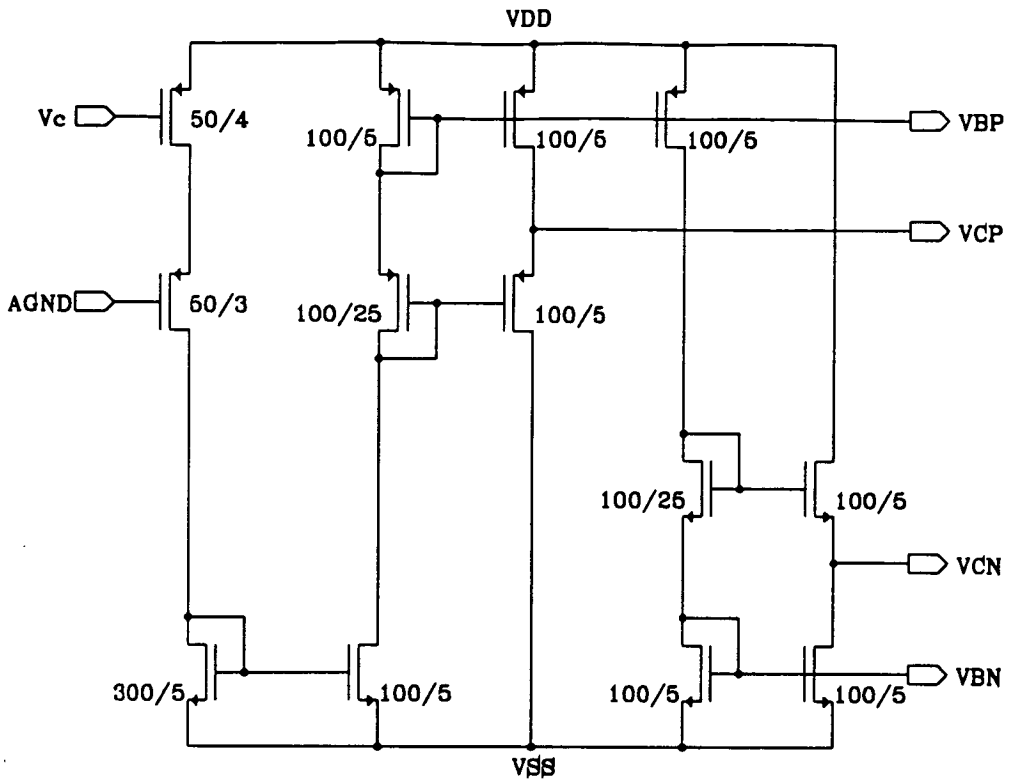


Figure 5.2-9 Bias circuit for grounded quad folded cascode transconductor

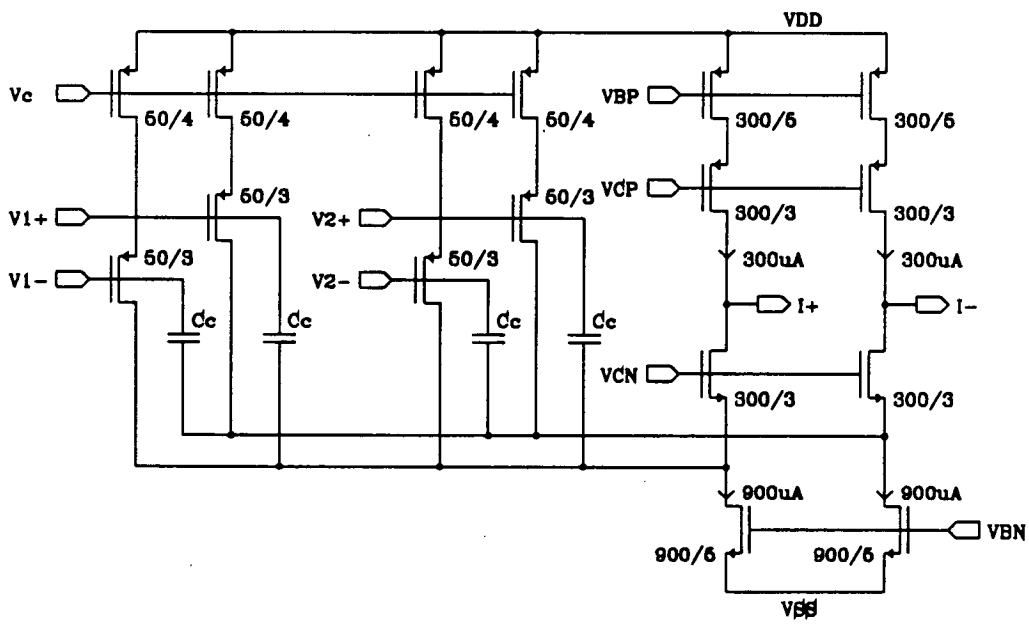


Figure 5.2-10 Double input folded cascode transconductor

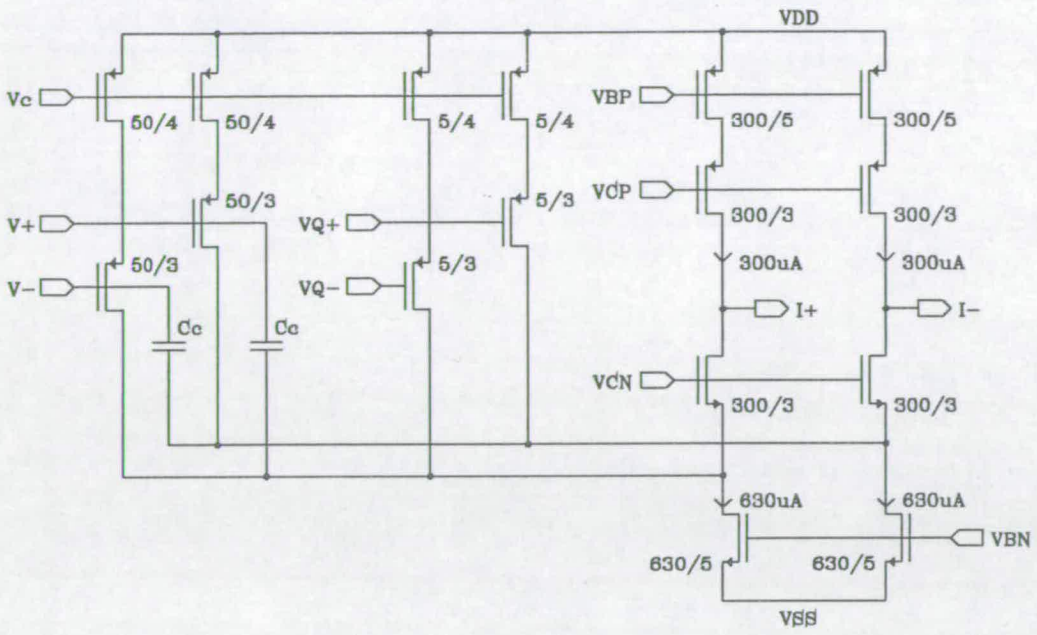


Figure 5.2-11 Folded cascode transconductor with 10:1 ratioed inputs

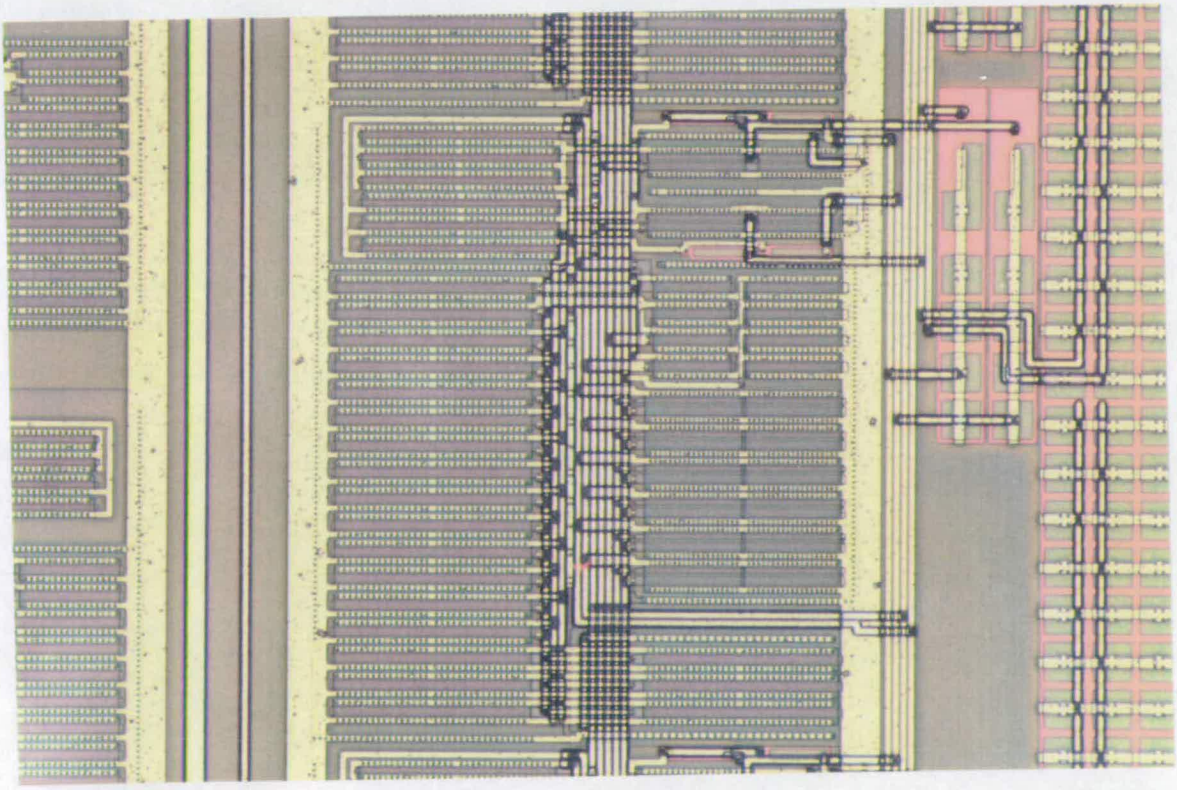


Figure 5.2-12 Photomicrograph of double input folded cascode transconductor

5.3 Low impedance inputs

As demonstrated in chapter 3, a ladder filter is formed by the interconnection of first order building blocks. The simplest first order section is the integrator with summing inputs, whose transfer function is

$$V_{out} = \frac{1}{sC}\sum_{i} V_i g_i \cdot \qquad (5.3\text{-}1)$$

This is realised by a set of transconductors of values g_i, whose outputs are connected to a common load capacitance C, driven by input voltages V_i.

The summing integrator described by 5.3-1 can be used alone only for a restricted class of filter responses. For more general application the first order building block requires non-integrating terms and takes the form:

$$V_{out} = \frac{1}{sC}\left[\sum_{i} V_i g_i + \sum_{j} C_j V_j\right] \qquad (5.3\text{-}2)$$

As explained in chapter 3, it is desirable that only one value of g_i be used in a particular filter. Where more than one value is used, the values should be in low integer ratios.

The non-integrating terms in (5.3-2) are realised by the use of input capacitors. There are three ways in which these input capacitors may be introduced into a first order section.

One of these methods is possible using conventional transconductors alone. This is to connect capacitors directly between the inputs and the output of the stage as shown in figure 5.3-1. It has the advantage of simplicity and there is negligible phase error associated with the non-integrating inputs. However since most of the input voltages V_j will be from the high impedance outputs of other transconductors (the obvious exception being the filter input itself) the capacitors C_j can usually form only bidirectional coupling paths. In the matrix formalism to be introduced in chapter 6, such paths are represented by the off-diagonal terms in symmetric matrices. In effect this means that C_j can implement only the (non-grounded) reactive components of the passive prototype. For bandpass filters this is a serious restriction since it is desirable to implement the termination resistors with capacitors in the active circuit to avoid the need for ratioed transconductors. It should be noted that in figure 5.3-1 the coupling capacitors contribute to the load of the integrator, and the sum of their values must be

subtracted from the value of the explicit load capacitor.

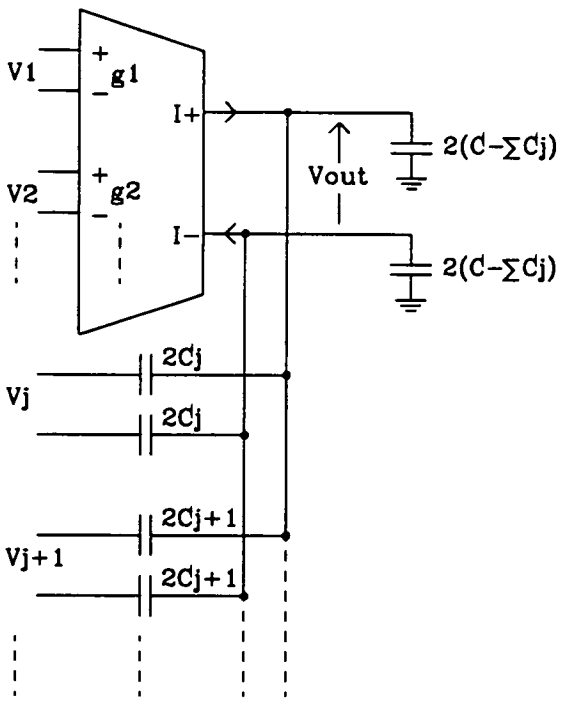


Figure 5.3-1 First order stage using conventional transconductor

One way to make the non-integrating inputs unidirectional is to buffer the input voltages V_j before they are applied to the capacitors C_j, as illustrated in figure 5.3-2. This method appears promising and such buffers are used routinely in bipolar circuits to drive the bases of transconductor input transistors [55]. The apparent drawback for a CMOS circuit is that even the simplest buffer such as a source follower will introduce several degrees of phase shift at high frequencies which can distort the response of the filter [27]. However if the use of buffers is limited to the termination branches, the effect of this phase shift can be negligible. This is demonstrated by the measured results for filter BPF2 in chapter 7.

A more elegant way to make the input capacitors unidirectional is to use transconductors with low impedance inputs, as shown in figure 5.3-3. In such circuits the output current is the sum of that from one or more conventional high impedance transconductive input, g_i, and that from an arbitrary number of capacitors connected between input voltages and a pair of current summing input nodes (denoted Z+ and Z-). These nodes have a similar function to the virtual earth of a conventional opamp stage or the X input of a current conveyor [72], though in this case the d.c. level will not usually equal that of the signal ground and is not in fact significant. The facility to include low impedance inputs with only a few additional components is one of the

attractions of using a FC transconductor. It opens up a range of new and useful filter topologies, which are introduced in the following chapter.

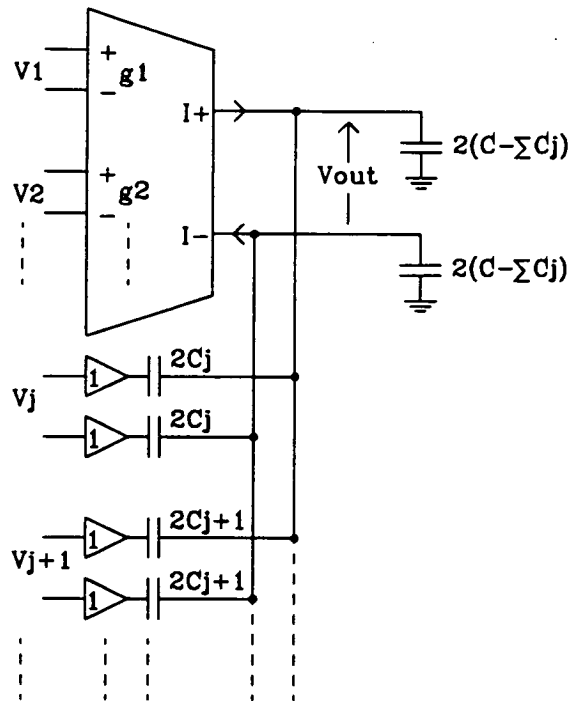


Figure 5.3-2 First order stage using transconductor and voltage buffers

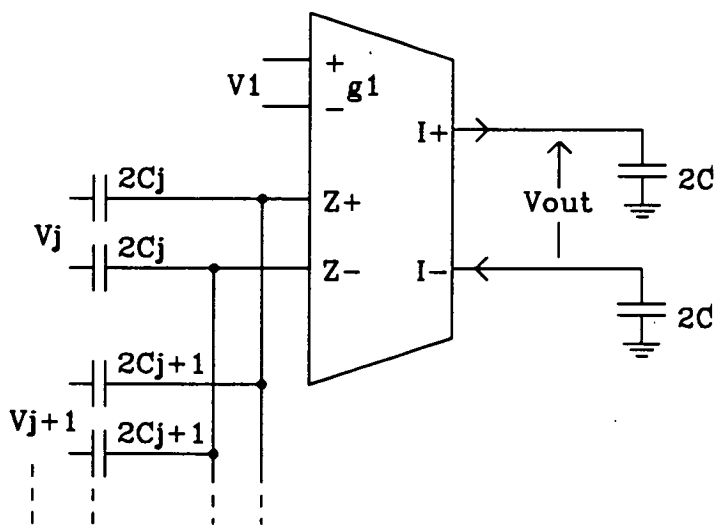


Figure 5.3-3

First order section using transconductor with low impedance inputs (Z+ and Z-)

Figure 5.3-4 shows how a low impedance input is included in one side of a FC circuit. The node used, Z+, is the drain of the n-type current source M_1. The impedance at this point in a conventional circuit (figure 5.2-3) is already moderately low since it is driven by the follower M_2. The voltage signal amplitude here is lower than at the output by one transistor gain. To decrease the impedance significantly, the bias voltage on the gate of M_2 is replaced by the output (V_2) of an inverting amplifier whose input is connected to the low impedance node. This amplifier can be a simple common source stage. Current injected into node Z+ tends to increase the voltage V_1. This causes a large decrease in V_2 which is followed by M_2 to oppose the increase in V_1.

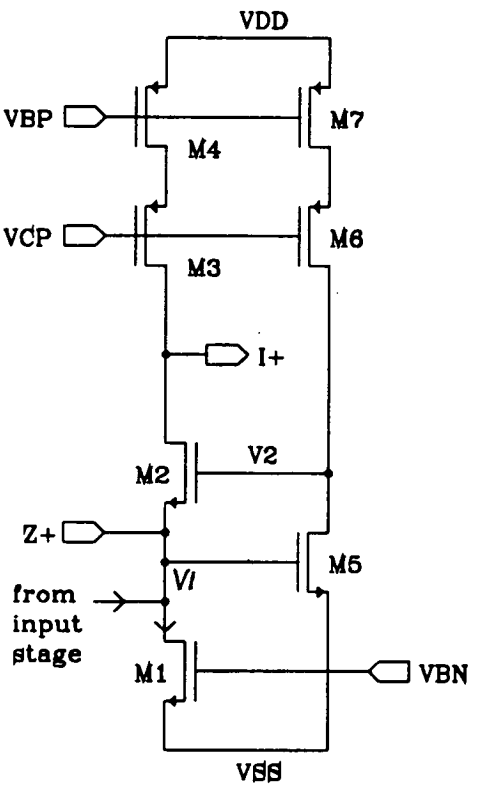


Figure 5.3-4 Introduction of a low impedance node to a folded cascode circuit

A small signal equivalent circuit of figure 5.3-4 is shown in figure 5.3-5. The terminology used is identical to that in figure 5.2-2, except that g_P is the output conductance of the p-type cascode current source (M_3 and M_4), g_A is the parallel output conductance of M_5 and its active load, and C_2 is the load capacitance seen by M_5, which is mostly due to the gate capacitance of M_2. There is now a significant capacitance, which we denote C_J, seen by the low impedance node due to the input capacitors C_j. However it is important to realise that

$$C_J < \sum_j C_j \qquad (5.3\text{-}3)$$

This is because the input capacitors are usually driven not by voltage sources but by current sources, i.e. other transconductors. The value of C_J depends on all the load capacitors connected to these transconductors and would be easy to calculate in a particular case if required.

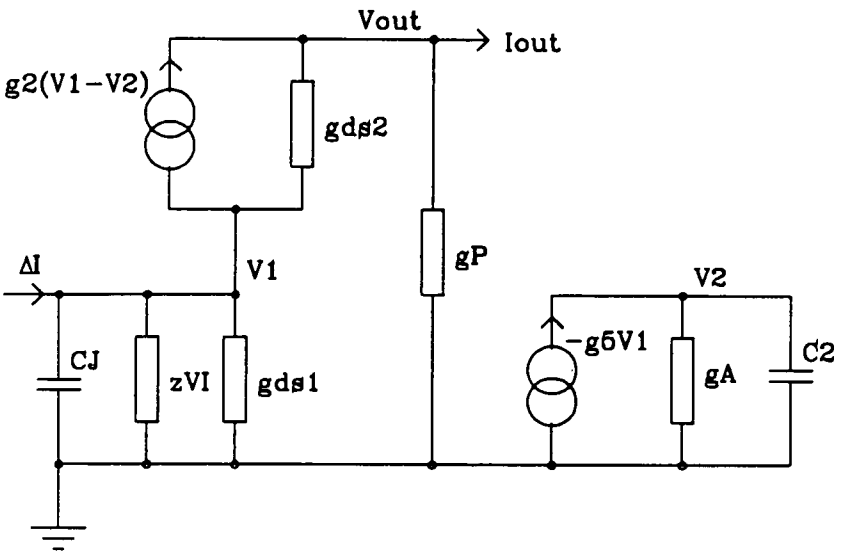


Figure 5.3-5 Small signal equivalent circuit of figure 5.3-4

ΔI now represents the total desired signal current entering the low impedance node, which we wish to transfer to the transconductor output, i.e.:

$$\Delta I = g_{in}V_{in} + s\sum_j V_j C_j \qquad (5.3\text{-}4)$$

as in (5.3-2).

We now calculate an expression for the transfer function of figure 5.3-5. The output current is

$$I_{out} = (g_{ds2}+g_2)V_1 - g_2V_2 - (g_{ds2}+g_P)V_{out} \qquad (5.3\text{-}5)$$

The transfer function of the inverter amplifier (M_5 plus load) is

$$V_2 = -\left(\frac{g_5}{sC_2+g_A}\right)V_1 \tag{5.3-6}$$

We substitute (5.3-6) into (5.3-5) to give

$$I_{out} = \left(g_2+g_{ds2}+\frac{g_2g_5}{sC_2+g_A}\right)V_1 - (g_{ds2}+g_P)V_{out} \tag{5.3-7}$$

KCL is applied at the low impedance node to obtain:

$$\left(g_2+g_{ds2}+\frac{g_2g_5}{sC_2+g_A}+g_{ds1}+sC_J\right)V_1 = \Delta I+g_{ds2}V_{out} \tag{5.3-8}$$

V_1 can be eliminated from (5.3-7) and (5.3-8), giving

$$Iout = \left(\frac{g_2+g_{ds2}+\frac{g_2g_5}{sC_2+g_A}}{g_2+g_{ds2}+\frac{g_2g_5}{sC_2+g_A}+gds1+sC_J}\right)\Delta I$$

$$-\left(\frac{g_{ds2}(sC_J+g_{ds1})}{g_2+g_{ds2}+\frac{g_2g_5}{sC_2+g_A}+gds1+sC_J}+g_P\right)V_{out} \tag{5.3-9}$$

From (5.3-8) and (5.3-9) we obtain a simplified expression for the transfer function by making the assumptions that $|sC_2|>>g_A$ and $g_2>>g_{dsi}$:

$$I_{out} = \left(\frac{\frac{\omega_o}{s\frac{}{Q}+\omega_o{}^2}}{s^2+s\frac{\omega_o}{Q}+\omega_o{}^2}\right)(g_{in}V_{in}+s\sum C_jV_j) \tag{5.3-10}$$

where

$$\omega_o = \sqrt{\frac{g_2g_5}{C_2C_J}} \tag{5.3-11}$$

and

$$Q=\sqrt{\frac{g_5 C_J}{g_2 C_2}} \qquad (5.3\text{-}12)$$

For (5.3-10) to approximate to the desired transfer function (5.3-4), we require ω_o to be much higher in frequency than the filter passband. To meet this condition (5.3-11) implies that the values of g_2 and g_5 should be as high as possible. However it should be remembered that increasing the width of M_2 will also increase the value of C_2, therefore a high value of g_2 should be reached by using a short device and increasing the bias current as necessary. The quadratic denominator in (5.3-10) arises from the closed loop formed by M_2 and M_5. In order for this loop to be stable, its quality factor (Q) must not be too high. Since C_J will generally be an order of magnitude greater than C_2, (5.3-12) shows that the transconductance of the cascode transistor, g_2, should be somewhat greater than that of the inverter amplifier, g_5.

A value for the d.c. output impedance of the transconductor is found from (5.3-9) by letting s tend to zero, and retaining only the most significant terms:

$$Z_{out} = \left[\frac{g_{ds2} g_{ds1} g_A}{g_2 g_5} + g_P\right]^{-1} \qquad (5.3\text{-}13)$$

A comparison of (5.3-13) with (5.2-5) shows that the contribution of the the n-type transistors to the output conductance is reduced by the gain of the inverter amplifier, and so the output impedance is now dominated by that of the p-type current source:

$$Z_{out} \cong g_P^{-1}. \qquad (5.3\text{-}14)$$

The inclusion of the low impedance inputs therefore increases Z_{out} by a small factor ($\cong 2$). If desired, Z_{out} could be increased greatly by using additional inverters to generate the p-type cascode bias voltages actively.

It is interesting to calculate an expression for the impedance of the low impedance node. This can be done by eliminating V_{out} from (5.3-7) and (5.3-8), with the assumption that almost all of I_{out} enters a load capacitor:

$$\frac{V_Z}{\Delta I} = \left[\frac{\frac{s}{C_J}+\frac{g_A}{C_2 C_J}}{s^2+s\left[\frac{g_2}{C_J}+\frac{g_A}{C_2}\right]+\frac{g_2(g_2+g_A)}{C_2 C_J}}\right] \qquad (5.3\text{-}15)$$

$$\equiv \begin{cases} \dfrac{g_A}{g_2 g_5} & \text{for} \quad |s| << \dfrac{g_A}{C_2} \\ \dfrac{sC_2}{g_2 g_5} & \text{for} \quad \dfrac{g_A}{C_2} << |s| << \omega_o \\ \dfrac{1}{sC_J} & \text{for} \quad |s| >> \omega_o \end{cases} \tag{5.3-16}$$

We conclude that the impedance of node Z+ is reduced by a factor approximately equal to the gain of the inverter amplifier. For typical values (such as $g_2 \cong 100\mu S$, $C_2 \cong 1pF$, $|s| \cong 1Mrad/sec$) this gain and the impedance of Z+ are in the regions of 40dB and 100Ω respectively. For frequencies beyond the dominant pole of the inverter amplifier the impedance Z+ appears inductive, since the transconductances of M_2 and M_5 form a gyrator (section 3.2) with C_2 as its load.

As well as facilitating filter design, the low value of Z+ also improves the performance of the transconductor in several respects. More of the current ΔI is transferred to the output and the output impedance is increased.

The schematic of a complete folded cascode transconductor with low impedance inputs and a grounded quad high impedance input stage is shown in figure 3.3-6. This is used in one of the experimental filters (BPF3) described in chapter 7.

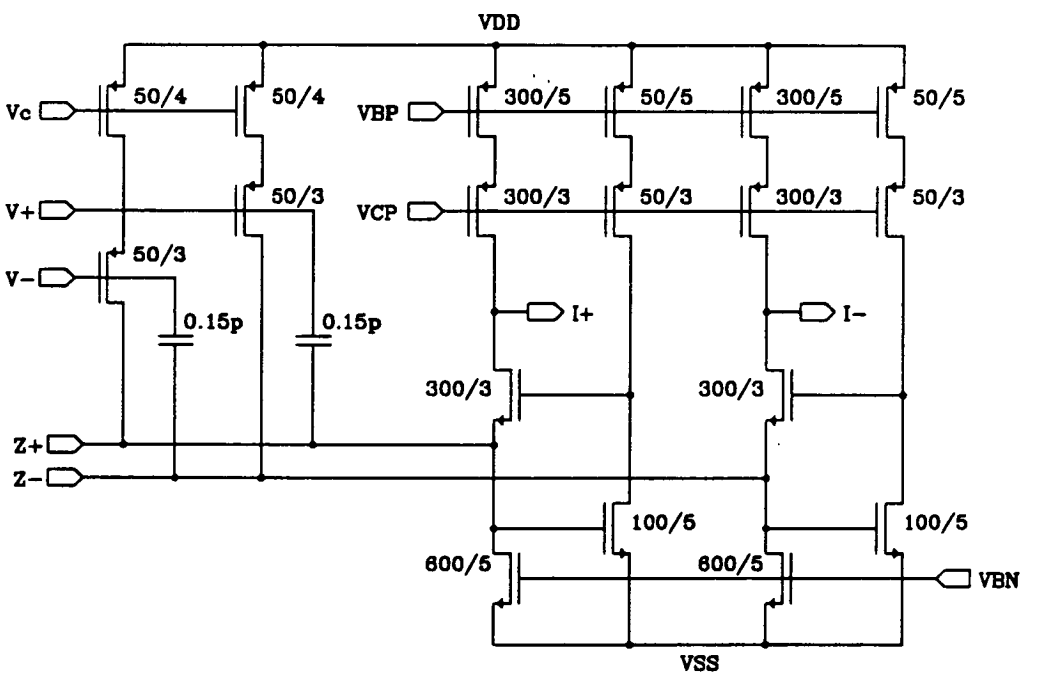


Figure 5.3-6 Fully differential transconductor with low impedance inputs

To illustrate the use of the low impedance inputs figure 3.3-7 shows an a.c. simulation of a first order stage configured as a 20dB attenuator, using the above transconductor with 79.6pF load capacitors and 7.96pF input capacitors. The phase response of this stage is flat to within 0.1^{o} from approximately 1 kHz to 1 MHz.

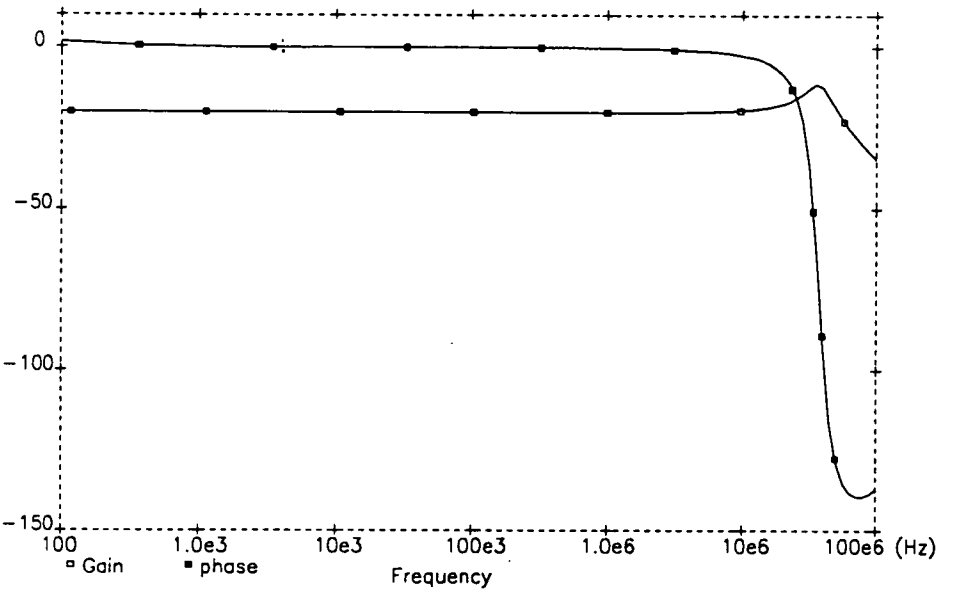


Figure 5.3-7 a.c. simulation of first order stage using transconductor of figure 5.3-6 configured for 20dB attenuation

5.4 A phase control technique

It is well known that the combined effect of parasitic poles in a transconductor can be cancelled to a large extent by the introduction of a left hand plane zero, often realised by a feedforward capacitor [20]. Such compensation can be introduced passively as in the transconductors shown so far in this chapter, e.g. figure 5.2-3; but for very selective filters the uncertainty in the frequency of the parasitic poles and the high sensitivity to phase error demand that active compensation be employed. In the circuit to be described the frequency of the zero is controlled by a d.c. voltage supplied to the transconductor. In a complete system this voltage could be generated by an amplitude lock loop [54].

The principle of the new technique is illustrated by the single ended equivalent circuit shown in figure 5.4-1.

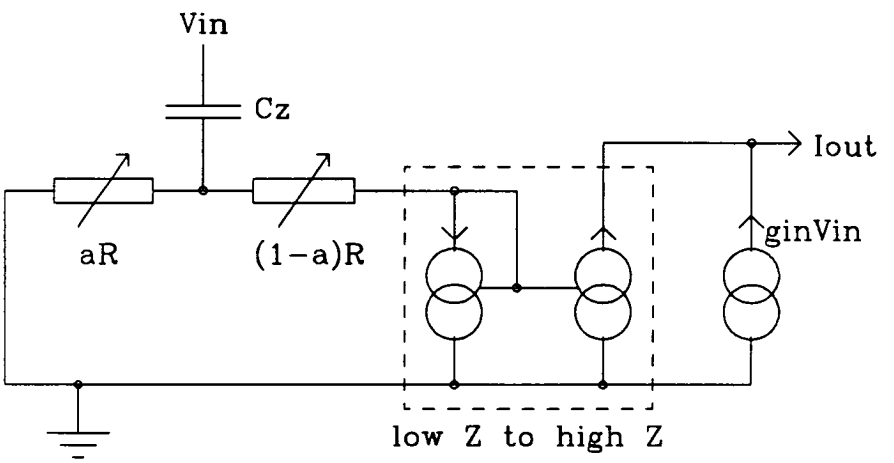


Figure 5.4-1 Variable phase compensation technique

The input voltage V_{in} is applied to a compensation capacitor C_z. The impedance of the two variable resistors is much less than that of C_z at the frequencies of interest, so their common node is at signal ground and the current in the capacitor is equal to sC_zV_{in}. The relative values of the resistors determine the fraction of this current, $(1\text{-}a)sC_zV_{in}$, which is shunted to ground. The remainder of the current, asC_zV_{in}, is passed to a low-to-high impedance converter at whose output it is summed with the conventional transconductor output, gmV_{in}. Therefore the total output current of the transconductor is:

$$I_{out} = gm\left[1-\frac{s}{z}\right]V_{in} \qquad (5.4\text{-}1)$$

where

$$z = -\frac{gm}{aC_z}. \qquad (5.4\text{-}2)$$

By adjusting the relative values of the resistors the frequency of the zero can be moved so that the best cancellation of parasitic poles is achieved.

Figure 5.4-2 shows the components needed to add the variable phase facility to a fully differential transconductor with low impedance inputs. These components replace the fixed capacitors in figure 5.3-6. Each variable resistor is implemented by a single MOSFET biassed in triode mode. The resistance of each of these transistors varies linearly with the applied gate voltage although in practice a monotonic relation would be sufficient. The phase control voltage V_q can be applied differentially about any common mode bias (such as midrail) which is sufficient to keep the transistors in triode mode over a large enough tuning range. A single ended V_q could also be applied with the other phase control input connected to midrail. Due to the symmetry of the fully differential circuit, the location of the compensating zero can be varied over a wide range of both positive and negative values; usually a negative value is required. The value of C_z is typically very small, since the parasitic poles are at very high frequencies. For this reason there is no problem satisfying the requirement that the impedance of the capacitor be much greater than that of the MOSFET variable resistors.

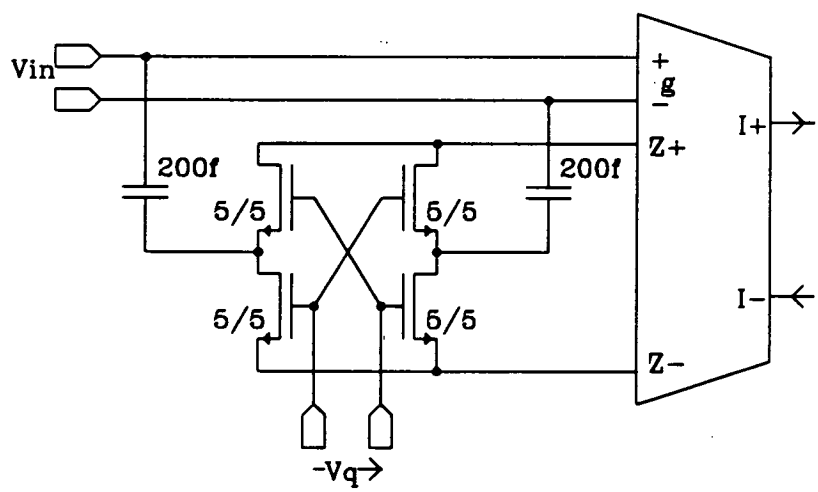


Figure 5.4-2 Addition of variable phase control to a fully differential transconductor with low impedance inputs

Figure 5.4-3 shows an a.c simulation of the variable phase transconductor for three values of Vq. There is a load capacitor of value 14.9pF on each output node, so

the unity gain frequency is 2MHz. With Vq=0, which is equivalent to no phase compensation circuit being present, the excess phase is 0.45°. With Vq=300mV the phase is overcompensated, giving a lead of 0.22°. Correct cancellation is achieved by Vq=150mV which gives an extremely flat phase response at the unity gain frequency. In fact the phase has a value of -90.00° from approximately 50kHz to 2.5MHz.

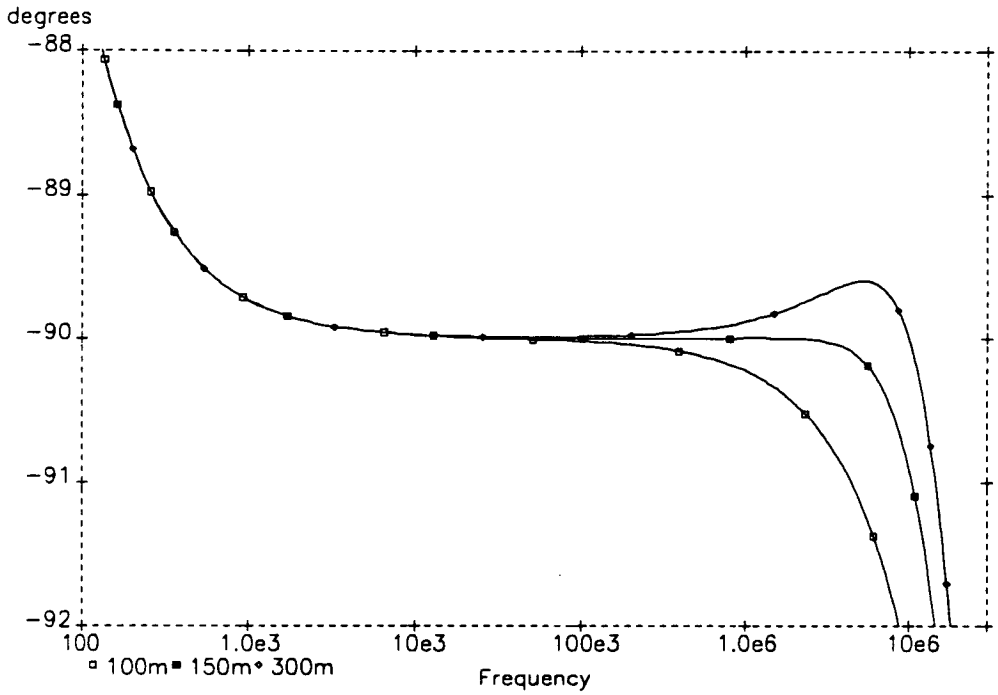


Figure 5.4-3

Simulated a.c. response of variable phase transconductor for different values of Vq.

Figure 5.4-4 illustrates how Q enhancement in a bandpass filter can be cancelled. The filter is the same as that shown in figure 3.2-23, but scaled to a centre frequency of 2MHz. The transconductor used in the simulation is a macromodel which includes a parasitic pole at 500MHz and the same phase correction components as shown in figure 5.4-2. The upper trace is the simulated response with Vq=0; this exhibits severe gain peaking at the passband edges due to excess phase in each integrator. The lower trace is the filter response with Vq=800mV (about a common mode of 2.5V); and in this case the transfer function is over damped. The middle trace shows that the Q-enhancement is cancelled accurately when Vq=500mV.

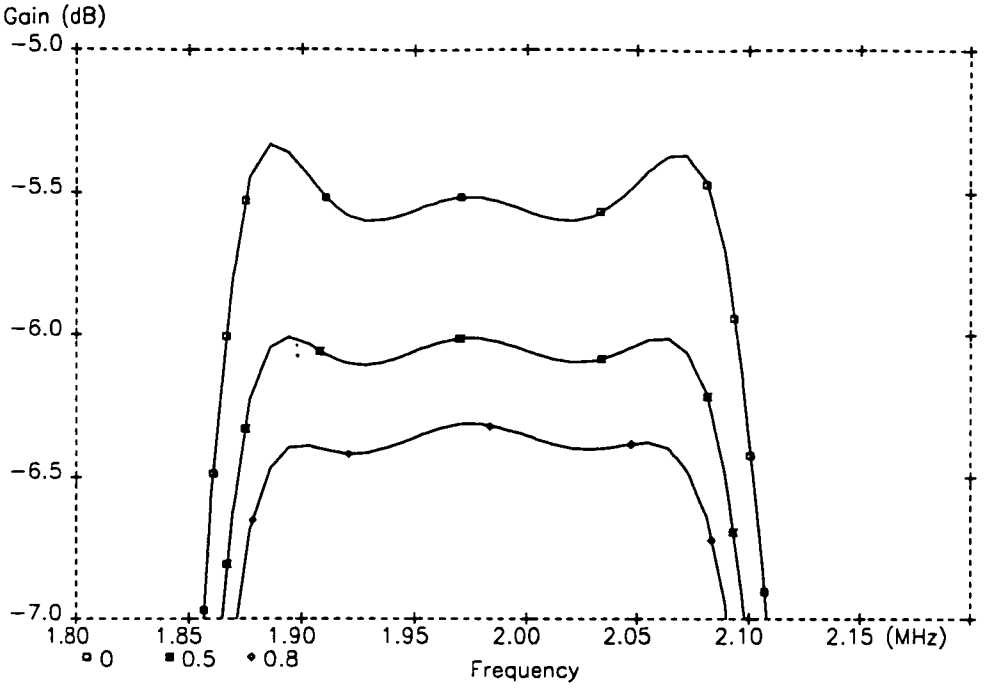


Figure 5.4-4 Simulated magnitude response of a sixth order bandpass filter using variable phase transconductor macromodels with three values of Vq.

CHAPTER 6
MATRIX METHODS FOR LADDER FILTER DESIGN

6.1 Introduction

In this chapter we present matrix based methods for the design of transconductor ladder filters, which can be applied to many more response types than the conventional methods described in chapter 3. The principal objective of this work is to be able to realise *any* passive ladder as a canonical transconductor filter using only a single value of transconductance, or a small number of values in simple integer ratios.

Matrix methods have already been developed for the design of switched capacitor and active-RC filters by Li, Henderson, and Sewell [61,62]. As well as formalising the design procedure and providing a framework for computer aided design tools [60], the use of matrices has facilitated the discovery of superior active filter structures which are far from intuitively obvious. The same advantages are found to apply for transconductor filters* .

The general procedure can be summarised as follows:

i. A set of equations (derived by Kirchhoff's laws) which describe the passive prototype are combined to form a matrix equation, second order in the Laplacian variable s:

$$\mathbf{J} = (\mathbf{G}+s\mathbf{C}+s^{-1}\mathbf{\Gamma})\mathbf{V} \qquad (6.1\text{-}1)$$

where **V** is a vector representing the nodal voltages (and/or branch currents) and **J** is a

*A completely different matrix based approach has also been used to derive alternative ladder structures and compare them with respect to sensitivity and scalability [58].

vector representing the input current source. **G**, **C**, and Γ are symmetric matrices whose elements are simple algebraic combinations of the passive component values.

ii. The nodal voltages of the prototype can be scaled if required by performing simple multiplication operations upon (6.1-1).

iii. The second order matrix equation is decomposed into two first order design equations by the introduction of a vector of auxiliary variables. A large number of decompositions are possible of which we present those most useful for transconductor filters. The choice of decomposition for a particular filter design is dictated by the type of building block available and the nature of the desired response. It should be appreciated that the number of decompositions suitable for transconductor filters is considerably smaller than for SC and RC filters. This is due to the reduction in degrees of freedom which results from restricting the number of transconductance values used in a particular filter.

iv. To form the active filter, each row of each design equation is implemented by one of the first order transconductor/capacitor sections which were described in section 5.3.

v. Finally the filter is scaled in frequency by the appropriate choice of transconductor and unit capacitor values.

In sections 6.2 to 6.6, this design procedure is discussed in detail for each commonly encountered type of filter response: lowpass, bandpass, highpass, bandstop and allpass.

The circuits described in this chapter have all been simulated or implemented fully differentially. This is to take advantage of the improved linearity, dynamic range, power supply rejection and high frequency performance that results from the symmetry of fully differential circuits. It also allows the realisation of negative capacitor values without the use of linear inverters, because the complement of each signal is already present in a fully differential circuit. However for clarity, single-ended versions of the filters are usually shown in this chapter. Fully differential schematics are given in the next chapter for the fabricated filters.

6.2 Lowpass ladders

A particular transfer function may be realised by many different RLC ladders and it is important to select a suitable one when designing an active filter. When the matrix methods described in this chapter are used, the main criterion is that the order of the matrices should be as low as possible. This is to minimise the number of variables simulated in the active ladder and hence ensure that it provides a canonical implementation of the transfer function. It is desirable that the active circuit be canonical (i.e. one first order section per filter pole) in order to minimise power consumption and circuit area.

For a particular RLC ladder there are also many different ways in which the matrices in (6.1-1) can be formulated. Again, the correct choice must be made to minimise the order of the active filter.

Fortunately the lowpass prototype ladders to be found in handbooks of filter tables are suitable for the design of transconductor ladders. As a first example we consider the prototype shown in figure 6.2-1. This topology can be used to realise a fifth order all-pole lowpass response (Butterworth, Chebyshev, Bessel etc). The values shown in the figure are for the Butterworth response, normalised to a -3dB cutoff frequency of 1 rad/sec.

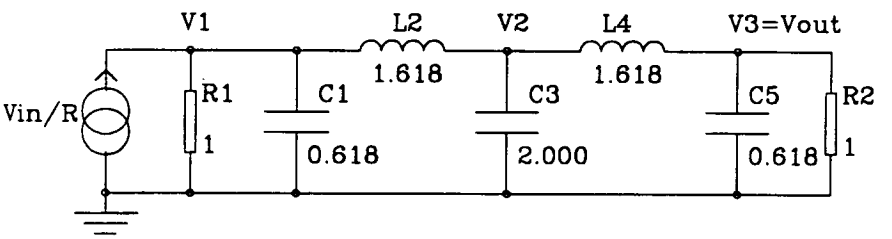


Figure 6.2-1 Fifth order Butterworth lowpass ladder

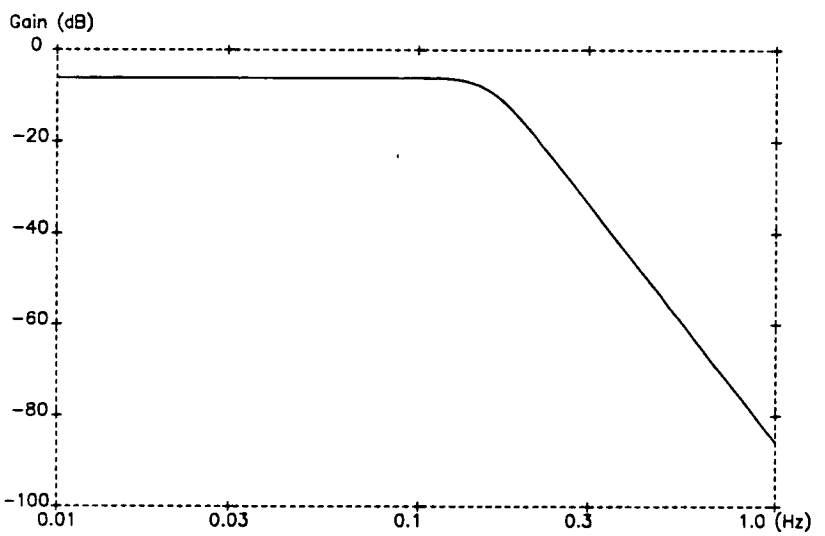


Figure 6.2-2 Amplitude response of fifth order Butterworth lowpass ladder

Applying Kirchhoff's current law (KCL) at each of the signal nodes gives the following equations:

$$\frac{V_{in}}{R_1} = V_1\left(\frac{1}{R_1}+sC_1+\frac{1}{sL_2}\right) - V_2\left(\frac{1}{sL_2}\right)$$

$$0 = -V_1\left(\frac{1}{sL_2}\right) + V_2\left(sC_3+\frac{1}{sL_2}+\frac{1}{sL_4}\right) - V_3\left(\frac{1}{sL_4}\right)$$

$$0 = -V_2\left(\frac{1}{sL_4}\right) + V_3\left(\frac{1}{R_2}+sC_5+\frac{1}{sL_4}\right). \qquad \text{(6.2-1a-c)}$$

These equations are identical to the matrix equation (6.1-1) if the vectors and matrices take the form:

$$\mathbf{J} = \begin{bmatrix} \frac{V_{in}}{R_1} \\ 0 \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, \qquad \mathbf{G} = \begin{bmatrix} \frac{1}{R_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{1}{R_2} \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_3 & 0 \\ 0 & 0 & C_5 \end{bmatrix}, \text{ and } \quad \Gamma = \begin{bmatrix} \frac{1}{L_2} & \frac{-1}{L_2} & 0 \\ \frac{-1}{L_2} & \frac{1}{L_2}+\frac{1}{L_4} & \frac{-1}{L_4} \\ 0 & \frac{-1}{L_4} & \frac{1}{L_4} \end{bmatrix}. \qquad \text{(6.2-2a-e)}$$

We refer to this as a "V representation", as the elements of **V** include only the *voltages* of the prototype.

For each prototype included in a filter table there are two versions: one with a minimum number of inductors and the other with a minimum of capacitors. It is interesting to demonstrate here that both versions can be represented by the same matrix equation. The minimum capacitance dual of the fifth order Butterworth lowpass ladder is shown in figure 6.2-3.

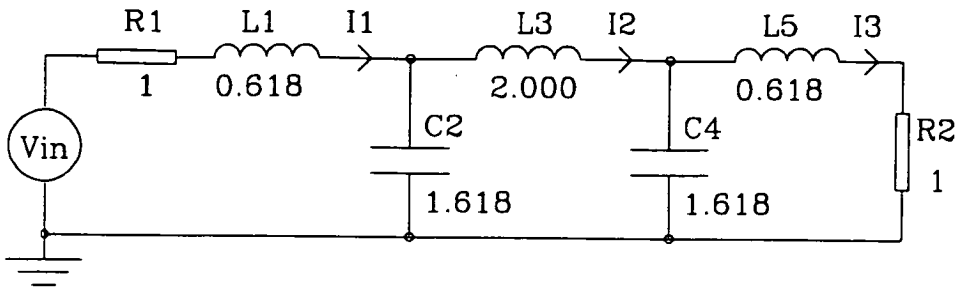


Figure 6.2-3 Fifth order Butterworth lowpass ladder with minimum capacitance

If the vector **V** for this ladder were composed of the nodal voltages then the matrices would be of fourth order. Instead we choose the currents in the inductors and apply Kirchhoff's voltage law:

$$V_{in} = I_1\left[R_1+sL_1+\frac{1}{sC_2}\right] - I_2\left[\frac{1}{sC_2}\right]$$

$$0 = -I_1\left[\frac{1}{sC_2}\right] + I_2\left[sL_3+\frac{1}{sC_2}+\frac{1}{sC_4}\right] - I_3\left[\frac{1}{sC_4}\right]$$

$$0 = -I_2\left[\frac{1}{sC_4}\right] + I_3\left[\frac{1}{R_2}+sL_5+\frac{1}{sC_4}\right]. \qquad (6.2\text{-}3a\text{-}c)$$

Strictly speaking **V** should include the output voltage (V_3) since this has to be simulated in the active circuit. However we do not have to include it explicitly in this case because I_3 is directly proportional to V_3, all of it passing through R_2. Equations (6.2-3a-c) are identical to (6.1-1) if the vectors and matrices now take the form:

$$\mathbf{J} = \begin{bmatrix} V_{in} \\ 0 \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}, \qquad \mathbf{G} = \begin{bmatrix} R_1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & R_2 \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_3 & 0 \\ 0 & 0 & L_5 \end{bmatrix}, \quad \text{and} \quad \Gamma = \begin{bmatrix} \frac{1}{C_2} & \frac{-1}{C_2} & 0 \\ \frac{-1}{C_2} & \frac{1}{C_2}+\frac{1}{C_4} & \frac{-1}{C_4} \\ 0 & \frac{-1}{C_4} & \frac{1}{C_4} \end{bmatrix}. \qquad (6.2\text{-}4a\text{-}e)$$

If the component values from figures 6.2-1 and 6.2-3 are substituted into (6.2-2a-e) and (6.2-4a-e) respectively, then the two sets of matrices are found to be the same.

We describe (6.2-4a-e) as an "I representation", since the elements of **V** include only the currents of the prototype. In the following sections we will also use "VI representations" in which the elements of **V** include both voltages and currents of the prototype.

We now consider how the transconductor ladder is derived from the matrix representation of the passive prototype. For lowpass filters this is best done by means of the Topological decomposition. If conventional transconductors are used this gives the same structures as would be obtained by leapfrog simulation or by the replacement of inductors by gyrators [section 3.2]. If transconductors with low impedance inputs are used, we obtain circuits which are insensitive to capacitor bottom plate parasitics.

Topological Decomposition

The inductor admittance matrix is factorised as:

$$\Gamma = \mathbf{A}\mathbf{D}\mathbf{A}^{T} \tag{6.2-5}$$

where **D** is a diagonal matrix whose order equals the number of inductors in the prototype and whose diagonal terms are the reciprocals of those inductances, and A_{ij} is an incidence matrix defined by:

$$A_{ij}^{T} = \begin{cases} -1 \text{ if branch i is incident upon and directed towards node j} \\ 0 \text{ if branch i is not incident upon node j} \\ 1 \text{ if branch i is incident upon and directed away from node j.} \end{cases} \tag{6.2-6}$$

We introduce a vector of auxiliary variables, defined by:

$$\mathbf{X} = (sg)^{-1}\mathbf{D}\mathbf{A}^{T}\mathbf{V} \tag{6.2-7}$$

where g is a factor with the dimensions of conductance, included to give **X** the dimensions of voltage, and (6.2-7) is substituted into (6.1-1) to obtain

$$\mathbf{C}\mathbf{V} = s^{-1}[\mathbf{J}-\mathbf{G}\mathbf{V}-g\mathbf{A}\mathbf{X}]. \tag{6.2-8}$$

Equations (6.2-7) and (6.2-8) are the two design equations for the Topological

decomposition. To obtain an active ladder, each row of these equations is realised by a first order transconductor section.

We illustrate the use of the Topological decomposition first for the prototype of figure 6.2-1. For this ladder:

$$\mathbf{D} = \begin{bmatrix} \frac{1}{L_2} & 0 \\ 0 & \frac{1}{L_4} \end{bmatrix}, \quad : \qquad \mathbf{A} = \begin{bmatrix} 1 & 0 \\ -1 & 1 \\ 0 & -1 \end{bmatrix} \tag{6.2-9a-b}$$

Substituting (6.2-2a-e) and (6.2-9a-b) into (6.2-7) and (6.2-8), and writing each row explicitly gives:

$$V_1 = \frac{g}{sC_1}[\alpha V_{in} - \alpha V_1 - X_1]$$

$$V_2 = \frac{g}{sC_3}[X_1 - X_2]$$

$$V_3 = \frac{g}{sC_5}[-\alpha V_3 + X_2]$$

$$X_1 = \frac{g}{sC_{L2}}[V_1 - V_2]$$

$$X_2 = \frac{g}{sC_{L4}}[V_2 - V_3] \tag{6.2-10a-e}$$

where

$$C_{Li} = g^2 L_i, \quad \text{for } i = 2,4 \tag{6.2-11}$$

and $$\alpha = \frac{1}{gR}. \tag{6.2-12}$$

Each of (6.2-10a-e) contains only integrated terms and can be realised by a simple summing integrator. This is because the **C** matrix is diagonal, which in turn is a consequence of the fact that the all-pole lowpass prototype contains only grounded capacitors. Combining these integrators gives the ladder shown in figure 6.2-4.

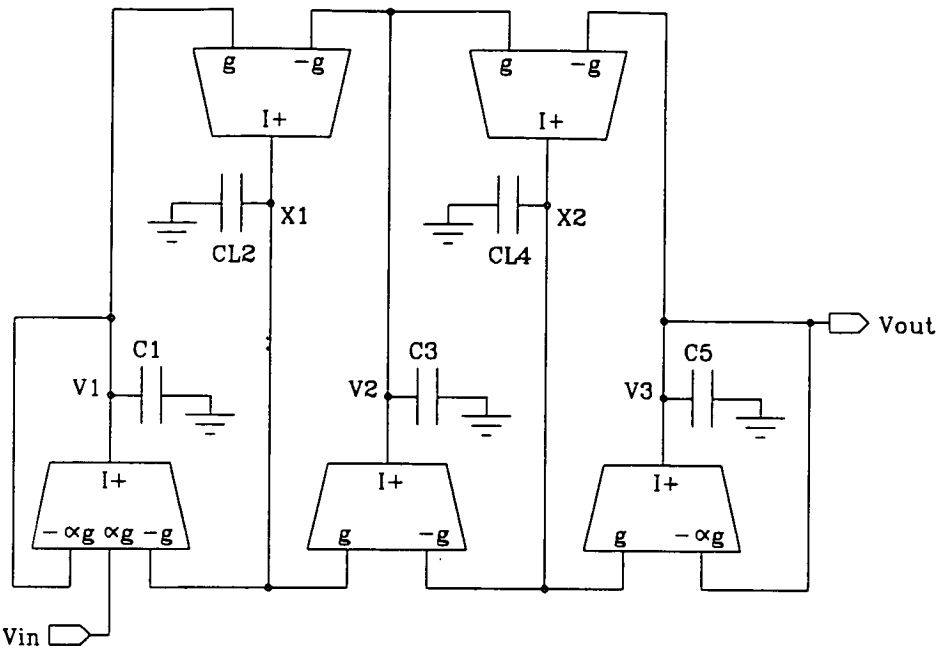


Figure 6.2-4 Fifth order Butterworth lowpass ladder

α is an arbitrary scaling factor whose value can be chosen to ensure that the peak amplitudes of the **V** and **X** voltages are as close as possible. In the ladder α represents the ratio of the transconductance used for the input and damping branches to that used in the rest of the ladder. For this reason it should have a simple rational value so that the different transconductances can be built from a unit value for best matching. Figures 6.2-5 and 6.2-6 show simulations of the transconductor ladder with two different values of α.

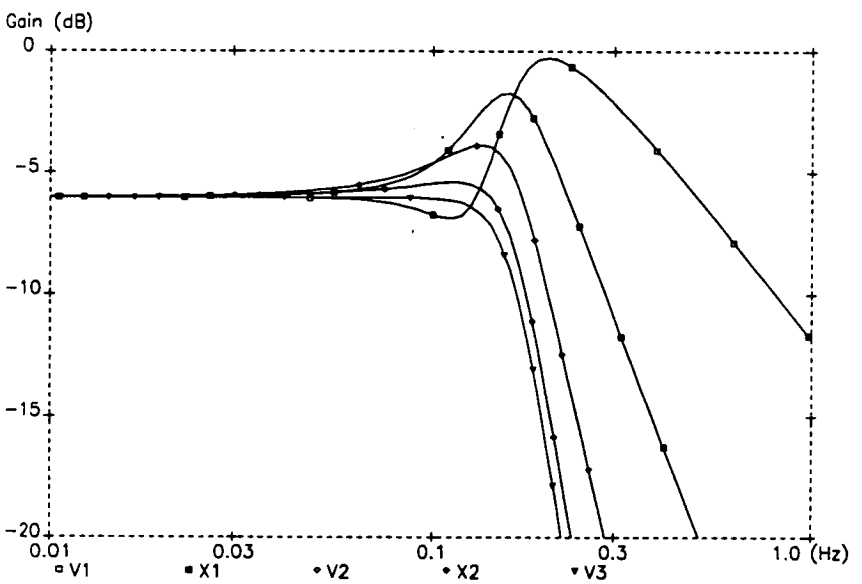


Figure 6.2-5 Simulation of Butterworth lowpass ladder with α=1

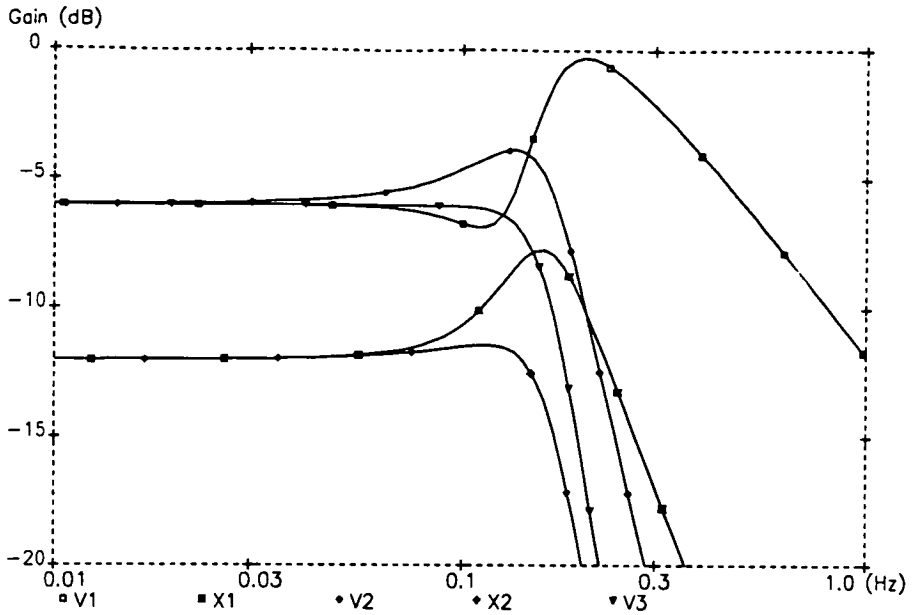


Figure 6.2-6 Simulation of Butterworth lowpass ladder with α=0.5

Clearly α=1 gives the best dynamic range scaling in this case. In general the optimum value of α depends on the particular transfer function being realised, however experience shows that for lowpass ladders the ratio is usually small. This observation may be attributed to the fact that lowpass filters inherently have a low selectivity.

Now we consider the design of lowpass ladders that include transmission zeros. As an example figure 6.2-7 shows a fifth order elliptic prototype with 0.1dB passband ripple and 69dB stopband attenuation. Figure 6.2-8 shows the ideal transfer function.

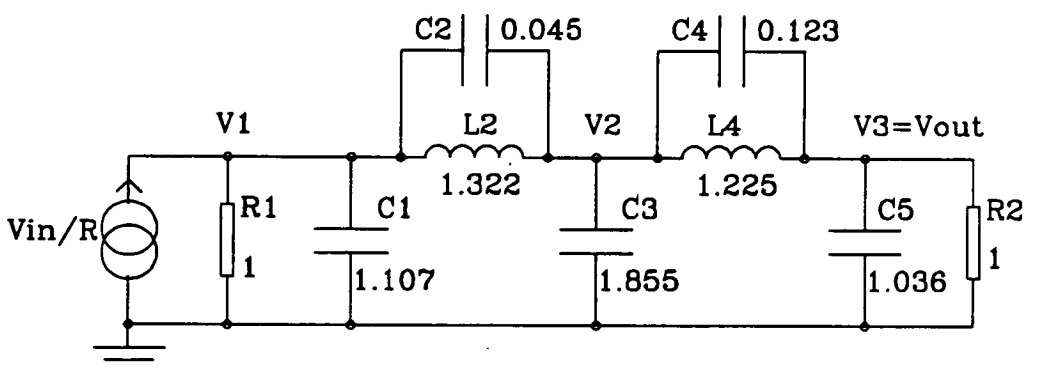


Figure 6.2-7 Fifth order elliptic lowpass RLC ladder

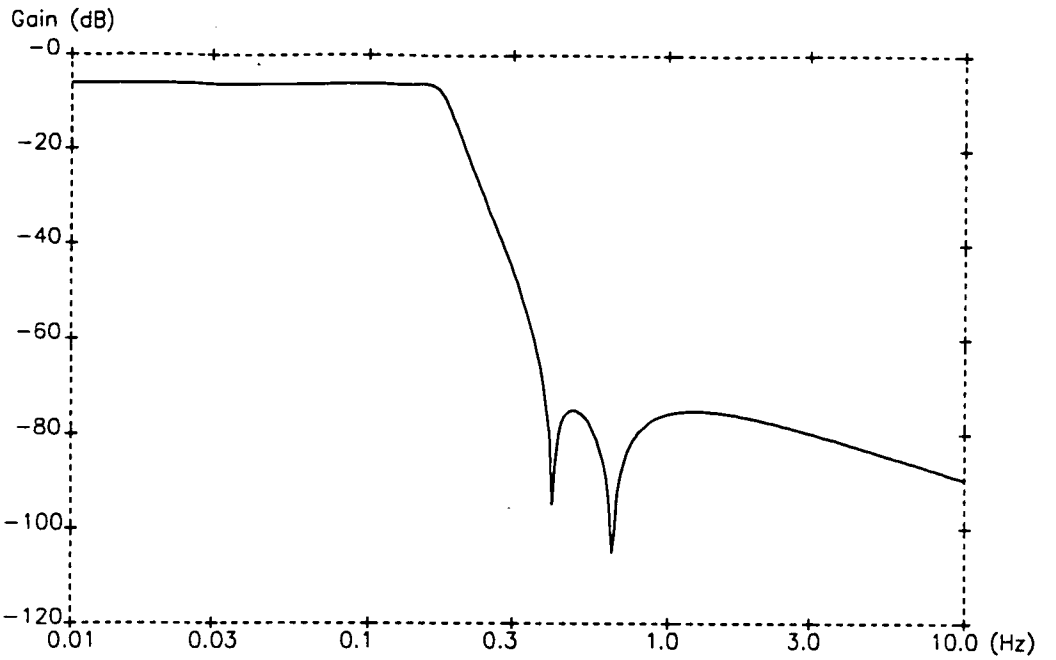


Figure 6.2-8 Magnitude response of fifth order elliptic lowpass ladder

Simulating the three signal nodes, this prototype is represented by equation (6.1-1) with the matrices

$$\mathbf{J} = \begin{bmatrix} \frac{V_{in}}{R} \\ 0 \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, \qquad \mathbf{G} = \frac{1}{R}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} C_1+C_2 & -C_2 & 0 \\ -C_2 & C_2+C_3+C_4 & -C_4 \\ 0 & -C_4 & C_4+C_5 \end{bmatrix}, \text{ and}$$

$$\Gamma = \begin{bmatrix} \frac{1}{L_2} & \frac{-1}{L_2} & 0 \\ \frac{-1}{L_2} & \frac{1}{L_2}+\frac{1}{L_4} & \frac{-1}{L_4} \\ 0 & \frac{-1}{L_4} & \frac{1}{L_4} \end{bmatrix}. \qquad \text{(6.2-13a-e)}$$

By applying the Topological decomposition and rearranging each row of the design equations resulting from (6.2-7 and 6.2-8), we find the equations for the five first order sections which form the active ladder:

$$V_1 = \frac{g[V_{in}-V_1-X_1]+sC_2V_2}{s(C_1+C_2)}$$

$$V_2 = \frac{g[X_1-X_3]+sC_2V_1+sC_4V_3}{s(C_2+C_3+C_4)}$$

$$V_3 = \frac{g[-V_3+X_3]+sC_4V_2}{s(C_4+C_5)}$$

$$X_1 = \frac{g}{sC_{L2}}[V_1-V_2]$$

$$X_2 = \frac{g}{sC_{L4}}[V_2-V_3] \qquad \text{(6.2-14a-e)}$$

where C_{Li} and α are as defined in (6.2-11) and (6.2-12). These equations differ from the corresponding equations in the previous example in that they include non-integrating terms. These are due to the floating capacitors (C_2 and C_4) which introduce non-diagonal elements in the **C** matrix. To realise them, first order transconductor-C sections corresponding to equation (5.3-2) must be used. Since the **C** matrix is always symmetric, each capacitor in the prototype can be implemented by a single capacitor in the active circuit (or two if fully differential) acting as a bidirectional coupling path (figure 5.3-1). Figure 6.2-9 shows the elliptic filter realised in this way with conventional transconductors. The drawback of this circuit is that the bottom plate parasitic associated with each floating capacitor is effective and must be compensated for by adjusting the value of the designed capacitor in parallel with the parasitic. As well as complicating the design procedure, this is likely to be problematic if the parasitic capacitance has not been determined accurately for the process concerned.

The problem of bottom plate parasitics can be overcome by the use of transconductors with low impedance inputs [63,73]. In this case each floating capacitor in the prototype is implemented as two capacitors in the active circuit (four if fully differential) and each bottom plate can be connected to a low impedance node (ground or a Z input) effectively shorting out the parasitics. Figure 6.2-10 shows the fifth order elliptic lowpass ladder which uses this method.

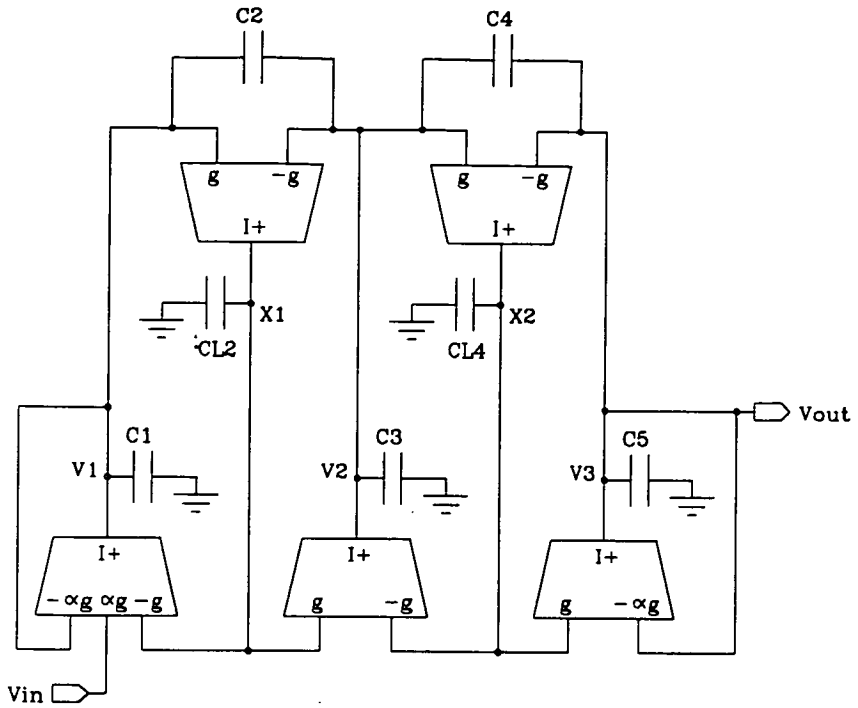


Figure 6.2-9 Fifth order lowpass elliptic ladder using conventional transconductors

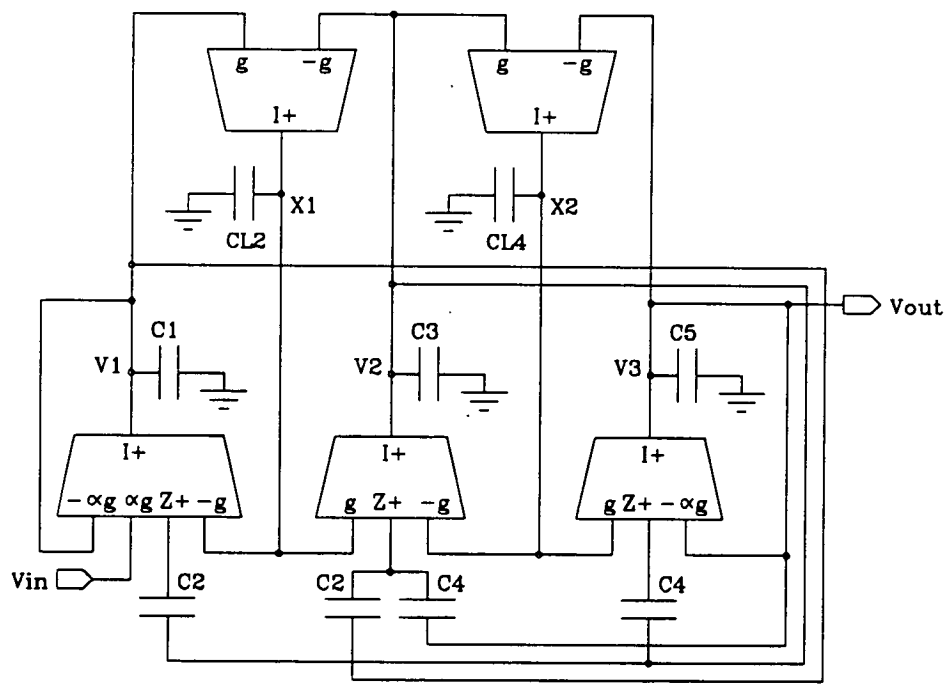


Figure 6.2-10 Fifth order lowpass elliptic ladder using transconductors with low impedance inputs

It will be clear from the examples given in this section that the Topological decomposition is a formal method of designing lowpass ladders, most of which can equally well be derived by "leapfrog" simulation as described in chapter 3. This section was included as an introduction to the matrix approach and to the use of transconductors with low impedance inputs. In contrast, the bandpass design methods introduced in the next section lead to original active filter structures. These overcome the problems that are encountered when attempting to design bandpass transconductor ladders using conventional coupled biquad techniques.

6.3 Bandpass ladders

In this section three decompositions are introduced and applied to the design of bandpass transconductor ladders. The decomposition applied in a particular case is determined by three factors: the type of prototype, the way in which the matrices describing the prototype are formulated, and the type of transconductor used to form the active circuit.

First we consider classical all-pole responses (Butterworth, Bessel, Chebyshev, etc), then classical responses with transmission zeros in the stopband (elliptic and inverse Chebyshev) and finally prototypes with non-classical transfer functions.

Figure 6.3-1 shows the prototype for a sixth order Chebyshev bandpass filter with 0.1dB passband ripple and a centre frequency of 1rad/sec. This was obtained from a third order lowpass ladder, using the standard frequency transformation equations. The gains from the input to the three nodes are shown in figure 6.3-2.

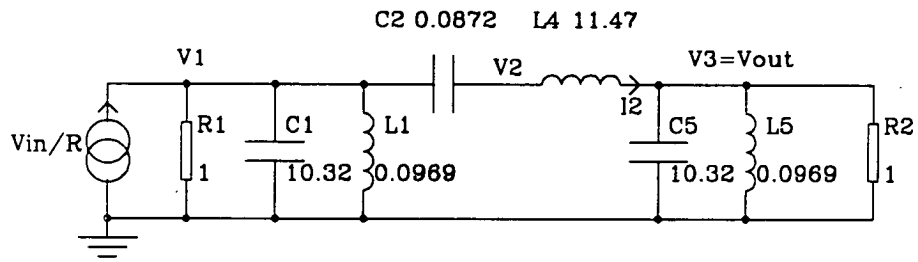


Figure 6.3-1 Sixth order Chebyshev bandpass RLC ladder

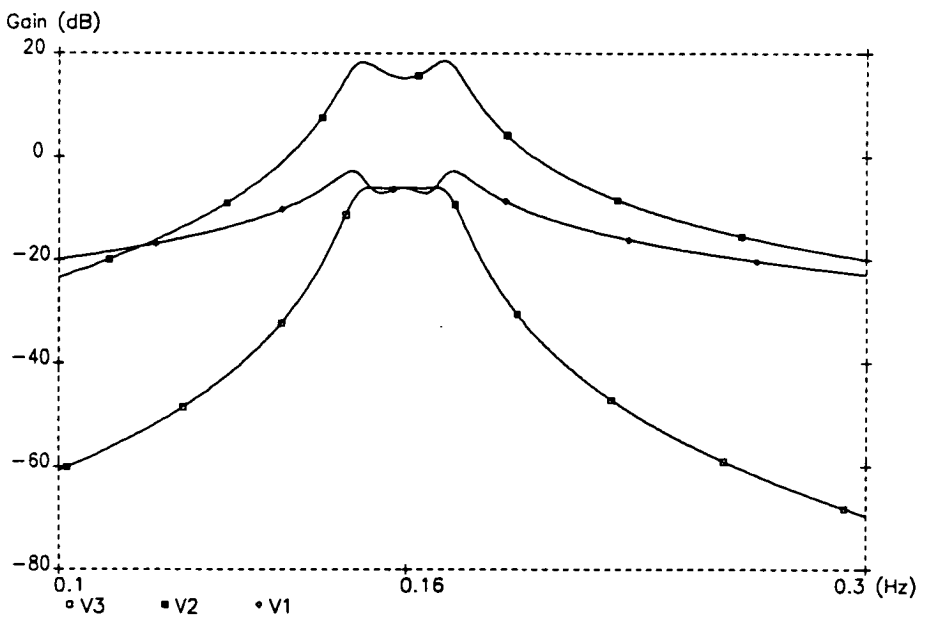


Figure 6.3-2 Nodal voltages of sixth order Chebyshev bandpass ladder

There are two ways in which the matrices describing this ladder can usefully be constructed, arising from different choices of variables to form the **V** vector. First we choose the nodal voltages V_1 and V_3, and the current I_2 passing through C_2 and L_2. This is a "VI representation". In order to preserve the consistency of dimensions we use a voltage variable V_{I2} proportional to I_2 (by a factor equal to the terminating resistance R). Applying KCL at nodes 1 and 3, and KVL around the middle loop gives:

$$\frac{V_{in}}{R_1} = V_1\left(\frac{1}{R_1}+sC_1+\frac{1}{sL_1}\right) + \frac{V_{I2}}{R}$$

$$0 = \frac{V_1}{R} - \frac{V_{I2}}{R^2}\left(sL_2+\frac{1}{sC_2}\right) - \frac{V_3}{R}$$

$$0 = -\frac{V_{I2}}{R} + V_3\left(\frac{1}{R_2}+sC_5+\frac{1}{sL_4}\right). \qquad (6.3\text{-}1a\text{-}c)$$

These equations equal the three rows of (6.1-1) if the matrices take the form:

$$\mathbf{J} = \begin{bmatrix} \frac{V_{in}}{R} \\ 0 \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_{I2} \\ V_3 \end{bmatrix}, \qquad \mathbf{G} = \frac{1}{R}\begin{bmatrix} 1 & 1 & 0 \\ 1 & 0 & -1 \\ 0 & -1 & 1 \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} C_1 & 0 & 0 \\ 0 & \frac{-L_4}{R^2} & 0 \\ 0 & 0 & C_5 \end{bmatrix}, \qquad \mathbf{G} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{-1}{R^2C_2} & 0 \\ 0 & 0 & \frac{1}{L_5} \end{bmatrix}. \qquad (6.3\text{-}2a\text{-}e)$$

Now to obtain the transconductor ladder we introduce the Left Direct (LD) Decomposition.

Left Direct Decomposition

The vector of auxiliary variables **X** is defined by:

$$g\mathbf{X} = sC\mathbf{V}, \qquad (6.3\text{-}3)$$

Equation (6.3-3) is substituted into (6.1-1) to give

$$\mathbf{J} = \mathbf{GV} + g\mathbf{X} + s^{-1}\Gamma\mathbf{V} \tag{6.3-4}$$

and the design equations are obtained by rearranging (6.3-3) and (6.3-4):

$$\mathbf{CV} = s^{-1}g\mathbf{X} \tag{6.3-5}$$

$$\mathbf{X} = -(sg)^{-1}\Gamma\mathbf{V} - g^{-1}\mathbf{GV} + g^{-1}\mathbf{J}. \tag{6.3-6}$$

From (6.3-5) and (6.3-6) the principal features of the LD decomposition can be deduced. Firstly, the matrix Γ should be diagonal in order to avoid the requirement for summing integrators which would imply the use of randomly ratioed transconductor values. Secondly, the damping and coupling banches (as represented by the term $g^{-1}\mathbf{GV}$) are non-integrated. These branches are unidirectional, since they describe a dependence of $\mathbf{X}$ upon $\mathbf{V}$ which is not matched by an identical dependence of $\mathbf{V}$ upon $\mathbf{X}$. Therefore, as we are looking for an "open loop integrator" realisation of the filter (chapter 1), transconductors with low impedance inputs must be used.

For the matrices (6.3-2a-e), the LD design equations can written explicitly as:

$$X_1 = \alpha V_{in} - \alpha V_1 - \alpha V_{I2} - \left(\frac{g}{sC_{L1}}\right) V_1$$

$$X_2 = -\alpha V_1 + \alpha V_3 + \left(\frac{g}{sC_2}\right) V_{I2}$$

$$X_3 = \alpha V_{I2} - \alpha V_3 - \left(\frac{g}{sC_{L5}}\right) V_3$$

$$V_1 = \left(\frac{g}{sC_1}\right) X_1$$

$$V_{I2} = \left(\frac{-g}{sC_{L4}}\right) X_2$$

$$V_3 = \left(\frac{g}{sC_5}\right) X_3. \tag{6.3-7a-f}$$

where as before $\alpha = \frac{1}{gR}$ is a factor which is chosen to scale the two sets of voltages correctly with respect to each other. By implementing each of (6.3-7a-f) with a first order transconductor-C section we obtain the transconductor ladder, a single ended version of which is shown in figure 6.3-3. Here the value $\alpha = 0.1$ has been chosen, corresponding to g = 10, and then the whole filter has been rescaled back to an impedance of 1Ω (g=1S).

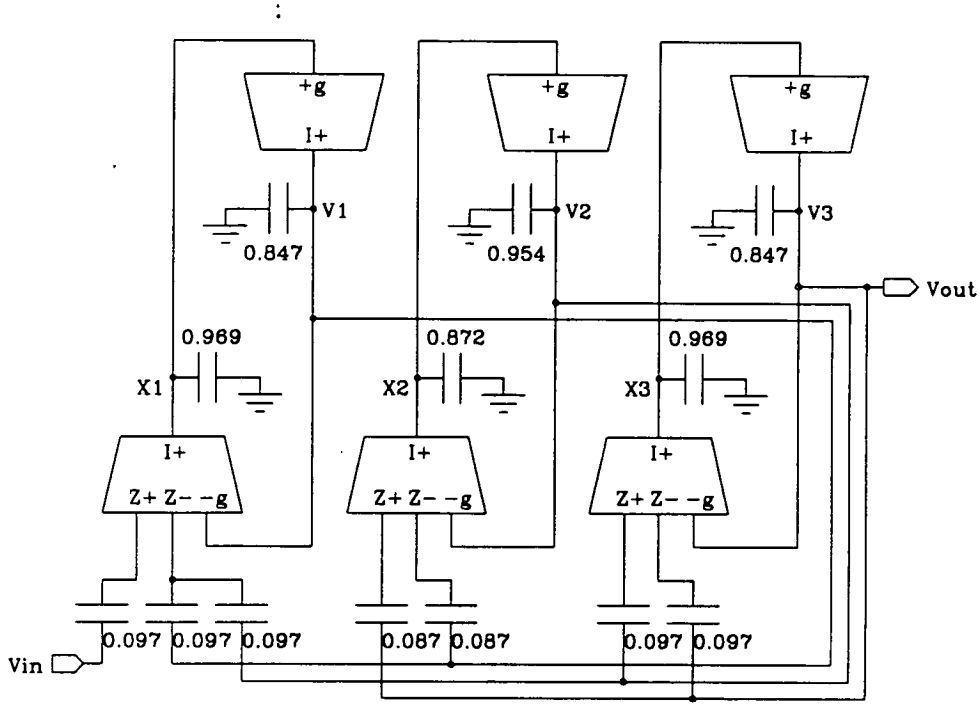


Figure 6.3-3 Sixth order Chebyshev bandpass filter (Left Direct decomposition)

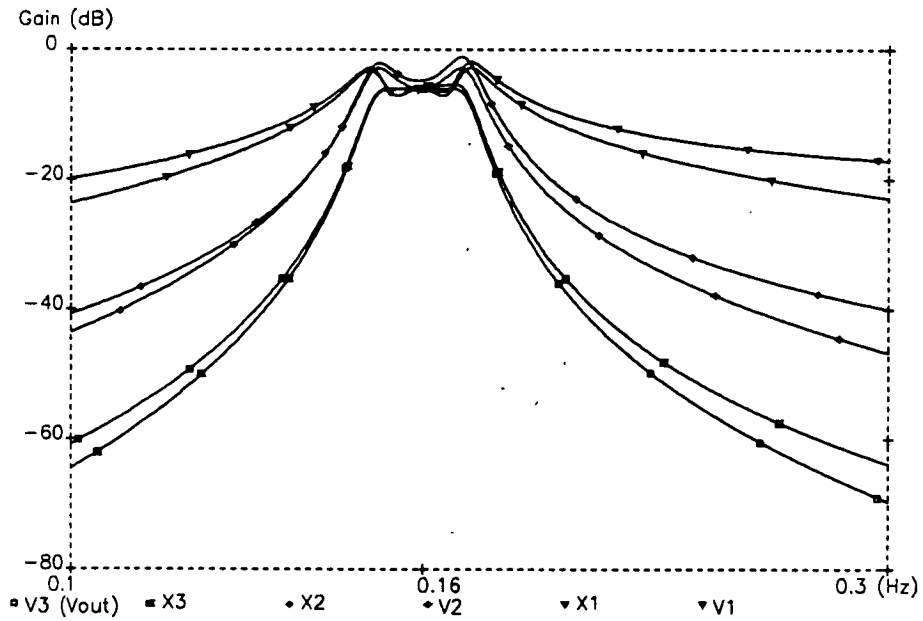


Figure 6.3-4 Simulation of Left Direct sixth order Chebyshev bandpass filter

Figure 6.3-4 shows the result of a SPICE simulation of the fully differential version of this circuit. The six curves are the outputs of the first order sections.

Now we consider the second way in which the matrices describing the all-pole prototype of figure 6.3-1 can be constructed. In this case the **V** vector is composed of the three nodal voltages of the prototype, giving a "V representation". By applying KCL at the three nodes and identifying the current conservation equations with (6.1-1) we find the matrices:

$$J = \begin{bmatrix} \frac{V_{in}}{R} \\ 0 \\ 0 \end{bmatrix}, \qquad V = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, \qquad G = \frac{1}{R}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix},$$

$$C = \begin{bmatrix} C_1+C_2 & -C_2 & 0 \\ -C_2 & C_2 & 0 \\ 0 & 0 & C_5 \end{bmatrix}, \qquad \Gamma = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_4} & \frac{-1}{L_4} \\ 0 & \frac{-1}{L_4} & \frac{1}{L_4}+\frac{1}{L_5} \end{bmatrix}. \qquad \text{(6.3-8a-e)}$$

The prototype of figure 6.3-1 cannot be implemented immediately using the V-representation because the middle node V_2 has a peak value significantly greater than the peak values of V_1 and V_3. This is illustrated in figure 6.3-2.

Before obtaining the active circuit it is necessary to attenuate V_2 without affecting the overall transfer function of the ladder. The matrix formulation allows this to be done very simply. If we wish to attenuate V_2 by a factor ν then we redefine V_2:

$$V_2 = \nu^{-1} V_2(\text{old}) \qquad \text{(6.3-9)}$$

For the matrix equation (6.1-1) to remain valid it is now necessary to multiply the second column of each of the matrices by ν, and to retain the symmetry of the matrices each second row is also multiplied by ν. After these operations, equations 6.3-8 become

$$\mathbf{J} = \begin{bmatrix} \frac{V_{in}}{R} \\ 0 \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, \qquad \mathbf{G} = \frac{1}{R}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} C_1+C_2 & -\nu C_2 & 0 \\ -\nu C_2 & \nu^2 C_2 & 0 \\ 0 & 0 & C_5 \end{bmatrix}, \quad \Gamma = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{\nu^2}{L_4} & \frac{-\nu}{L_4} \\ 0 & \frac{-\nu}{L_4} & \frac{1}{L_4}+\frac{1}{L_5} \end{bmatrix}. \qquad (6.3\text{-}10a\text{-}e)$$

The central elements of the matrices **C** and Γ are multiplied by ν^2 since they lie on the intersection of the second row and second column, and they are therefore no longer equal in magnitude to any adjacent elements. This implies that if we reconstruct a passive ladder from (6.3-10a-e), two new components have to be introduced (L_3 and C_3) so that the inductive and capacitive loads on node 2 no longer equal those on nodes 3 and 1 respectively. This modified ladder is given in figure 6.3-5 for $\nu = 10$. Figure 6.3-6 is a SPICE simulation of the modified ladder, which should be compared to figure 6.3-2.

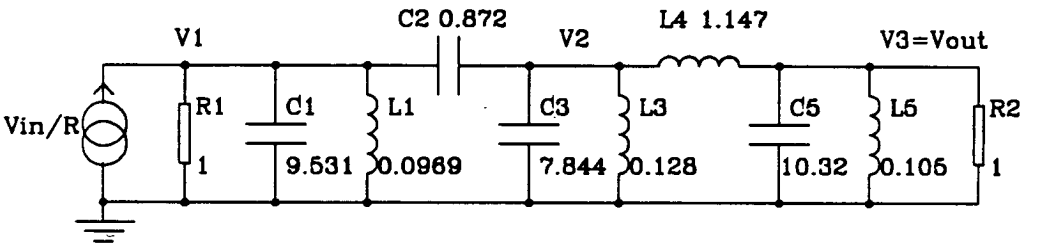


Figure 6.3-5 Sixth order all-pole bandpass passive ladder with nodal voltages scaled for correct dynamic range

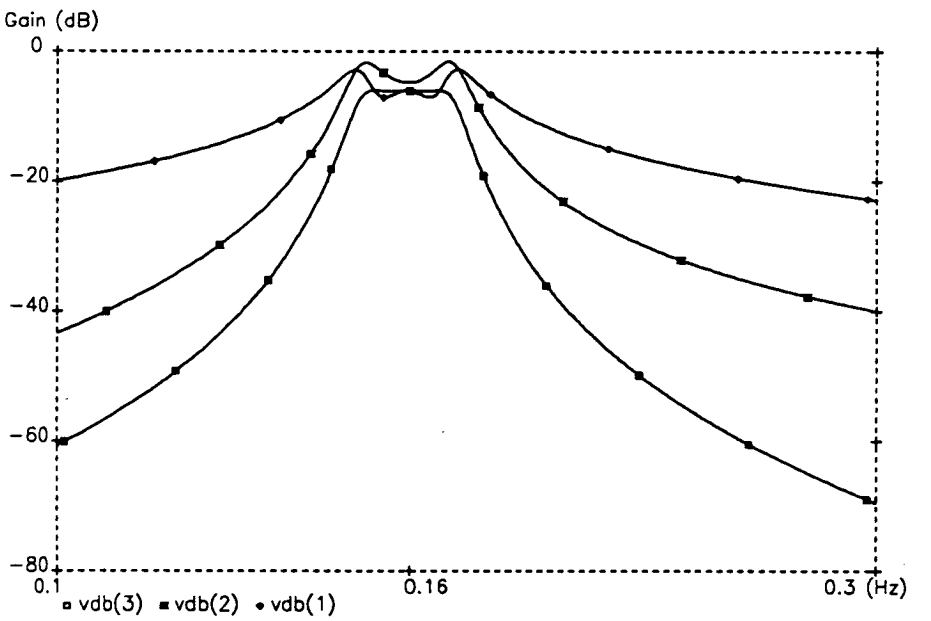


Figure 6.3-6 SPICE simulation of ladder in figure 6.3-5

Now we consider how an active circuit can be derived from the V-representation of the all-pole bandpass ladder. The Left Direct decomposition defined earlier in this section is unfortunately not suitable because one of the LD design equations (6.3-6) includes the term $(sg)^{-1}\Gamma\mathbf{V}$. This would have to be implemented using summing integrators with random transconductor ratios, since Γ is non-diagonal in the V-representation. However if equation (6.3-6) is premultiplied by the inverse of Γ then the integrated term contains only the vector **V**, and a single value of transconductance can then be used for all of the integrators. This technique, which we call the "Left Inverse (LI)" decomposition, illustrates the power of the matrix formalism. A very simple step in matrix algebra can be used to generate active circuits with specific desired features which could not be obtained using the more conventional methods described in chapter 3.

In fact there is a whole class of LI decompositions, which can be defined generally as follows:

Left Inverse Decomposition (General)
referring again to (6.1-1) we decompose **C** into the product of two matrices:

$$\mathbf{C} = \mathbf{C}_l\mathbf{C}_r. \tag{6.3-11}$$

The vector **X** of auxiliary voltage variables is defined by

$$\sigma\mathbf{X} = s\mathbf{C}_r\mathbf{V}. \tag{6.3-12}$$

where σ is a scaling factor whose dimensions are determined by the choice of $\mathbf{C}_r$. Substituting (6.3-11) and (6.3-12) into (6.1-1) gives

$$\sigma\mathbf{C}_l\mathbf{X} = \mathbf{J} - \mathbf{G}\mathbf{V} - s^{-1}\Gamma\mathbf{V}. \tag{6.3-13}$$

The general LI design equations are obtained by multiplying (6.3-13) by Γ^{-1}, and rearranging (6.3-12):

$$\sigma\Gamma^{-1}\mathbf{C}_l\mathbf{X} = \Gamma^{-1}\mathbf{J} - \Gamma^{-1}\mathbf{G}\mathbf{V} - s^{-1}\mathbf{V}. \tag{6.3-14}$$

$$\mathbf{C}_r\mathbf{V} = \sigma s^{-1}\mathbf{X}. \tag{6.3-15}$$

There are many LI decompositions, given by the different ways in which $\mathbf{C}_l$ and $\mathbf{C}_r$

can be chosen, subject to (6.3-11). However three general characteristics of LI filters can be observed from (6.3-14) and (6.3-15). Firstly, the two integrated terms never include premultiplying matrices, so only a single value of transconductance is ever needed. Secondly, some of the non-integrated terms give unidirectional coupling paths, so transconductors with low impedance inputs are required. Thirdly, the inverted matrix can often lose the sparsity of Γ (i.e. it can have few or no zero elements) and care must be taken in choosing the prototype and the form of $\mathbf{C}_l$ to avoid the transconductor ladder having an excessive number of capacitors.

To complete the design of the all-pole bandpass ladder with V representation, we define a specific LI decomposition.

Left Inverse Decomposition (Type 1)
In (6.3-11) we let

$$\mathbf{C}_l = \mathbf{I} \text{ (the identity matrix)}$$

and

$$\mathbf{C}_r = \mathbf{C}. \qquad (6.3\text{-}16a,b)$$

From (6.3-12) it can then be seen that this gives σ the dimensions of conductance, and for clarity we rename the scaling factor

$$g = \sigma. \qquad (6.3\text{-}17)$$

Substituting (6.3-16) and (6.3-17) into (6.3-14) and (6.3-15) gives the design equations for the LI (type1) decomposition:

$$g\Gamma^{-1}\mathbf{X} = \Gamma^{-1}\mathbf{J} - \Gamma^{-1}\mathbf{G}\mathbf{V} - s^{-1}\mathbf{V} \qquad (6.3\text{-}18)$$

$$\mathbf{C}\mathbf{V} = gs^{-1}\mathbf{X}. \qquad (6.3\text{-}19)$$

For the matrices defined in (6.3-10) the rows of the LI (type1) design equations are:

$$V_1 = \frac{1}{sC_{11}}[gX_1 - sC_{12}V_2]$$

$$V_2 = \frac{1}{sC_{22}}[gX_2 - sC_{21}V_1]$$

$$V_3 = \frac{1}{sC_{33}}[gX_3]$$

$$X_1 = \frac{1}{s(g^2L_{11})}[-gV_1+s(\alpha g^2L_{11})V_{in}-s(\alpha g^2L_{11})V_1]$$

$$X_2 = \frac{1}{s(g^2L_{22})}[-gV_2-s(\alpha g^2L_{23})V_3-s(g^2L_{23})X_3]$$

$$X_3 = \frac{1}{s(g^2L_{33})}[-gV_3-s(g^2L_{32})X_2-s(\alpha g^2L_{33})V_3]. \qquad (6.3\text{-}20a\text{-}f)$$

where C_{ij} and L_{ij} are elements of **C** and Γ^{-1} respectively. The inverse matrix can be computed using readily available routines [74].

In (6.3-20d-f) the products giving capacitor values are highlighted with curved brackets. Implementing each of (6.3-20) with the first order section (figure 5.3-3) gives the transconductor ladder a single ended version of which if shown in figure 6.3-7. We have chosen $\alpha = 0.1$, corresponding to g = 10, and then rescaled the filter back to an impedance of 1Ω (g=1S).

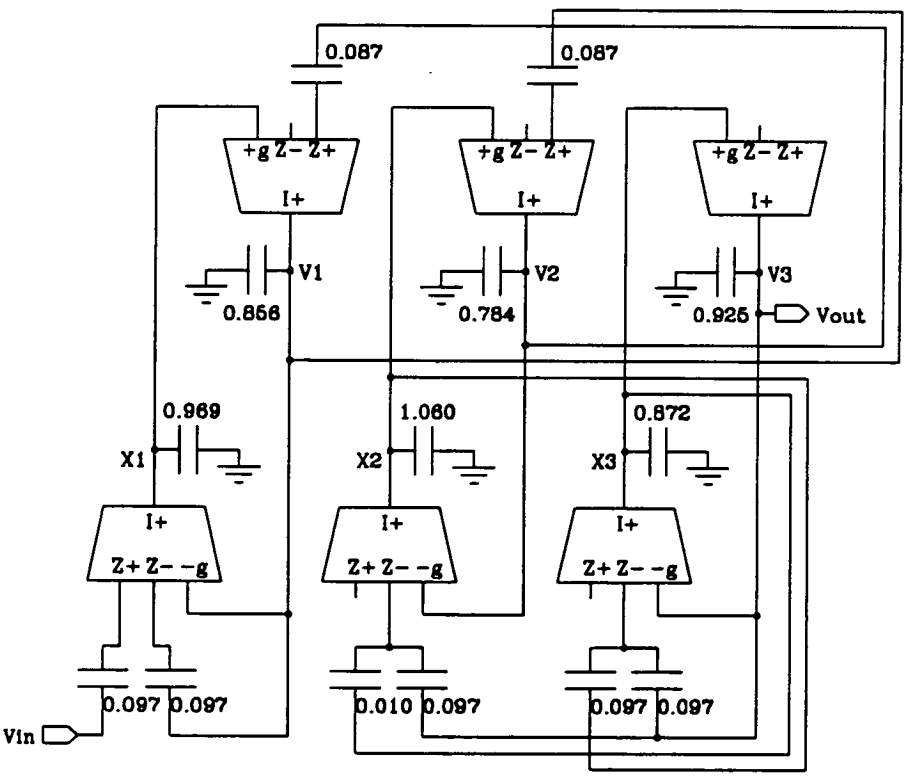


Figure 6.3-7 Sixth order Chebyshev ladder obtained by V-representation of prototype, LI (type1) decomp., and using transconductors with low impedance inputs.

A comparison of figures 6.3-3and 6.3-7 shows that the VI representation and the Left Direct decomposition give a slightly simpler active realisation of the sixth order symmetric all-pole bandpass response than the V representation with LI (type 1). Both circuits however have an acceptable level of complexity, and we will show that in general LI decompositions have greater applicability than the LD decomposition.

The choice between the V and VI representations becomes easier to make for bandpass filters derived from an *even* order lowpass prototype. Figure 6.3-8 shows an eighth order symmetric Butterworth bandpass prototype, obtained by transformation of a fourth order lowpass ladder.

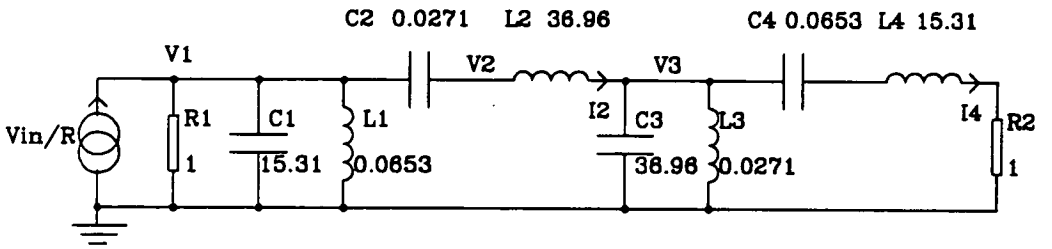


Figure 6.3-8 Eighth order Butterworth bandpass RLC ladder

This circuit has five nodes, so using the V representation would require fifth order matrices, which in turn would lead to a tenth order (i.e. non-canonical) transconductor filter. Instead we can construct the vector **V** from two nodal voltages (V_1 and V_3), and the currents through the two LC series branches (I_2 and I_4). As before we use voltages (V_{I2} and V_{I4}) proportional to the currents and the terminating resistance, in order to preserve dimensional consistency. It is not necessary to simulate the output voltage (V_5) of the passive ladder explicitly, because all of I_4 passes through the termination resistor and V_{I4} can therefore be treated as the output voltage. This was also the case in the I representation of the minimum capacitance lowpass ladder described in the previous section. For the VI representation of the eighth order Butterworth bandpass ladder the matrices are:

$$\mathbf{J} = \begin{bmatrix} \frac{V_{in}}{R} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_{I2} \\ V_3 \\ V_{I4} \end{bmatrix}, \qquad \mathbf{G} = \frac{1}{R}\begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & -1 & 1 \end{bmatrix},$$

$$C = \begin{pmatrix} C_1 & 0 & 0 & 0 \\ 0 & \frac{-L_2}{R^2} & 0 & 0 \\ 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & \frac{-L_4}{R^2} \end{pmatrix}, \quad \Gamma = \begin{pmatrix} \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{-1}{R^2C_2} & 0 & 0 \\ 0 & 0 & \frac{1}{L_3} & 0 \\ 0 & 0 & 0 & \frac{-1}{R^2C_4} \end{pmatrix}. \qquad \text{(6.3-21a-e)}$$

Substituting (6.3-21a-e) into the LD design equations gives the transconductor ladder shown in figure 6.3-9. A simulation of the fully differential version is shown in figure 6.3-10.

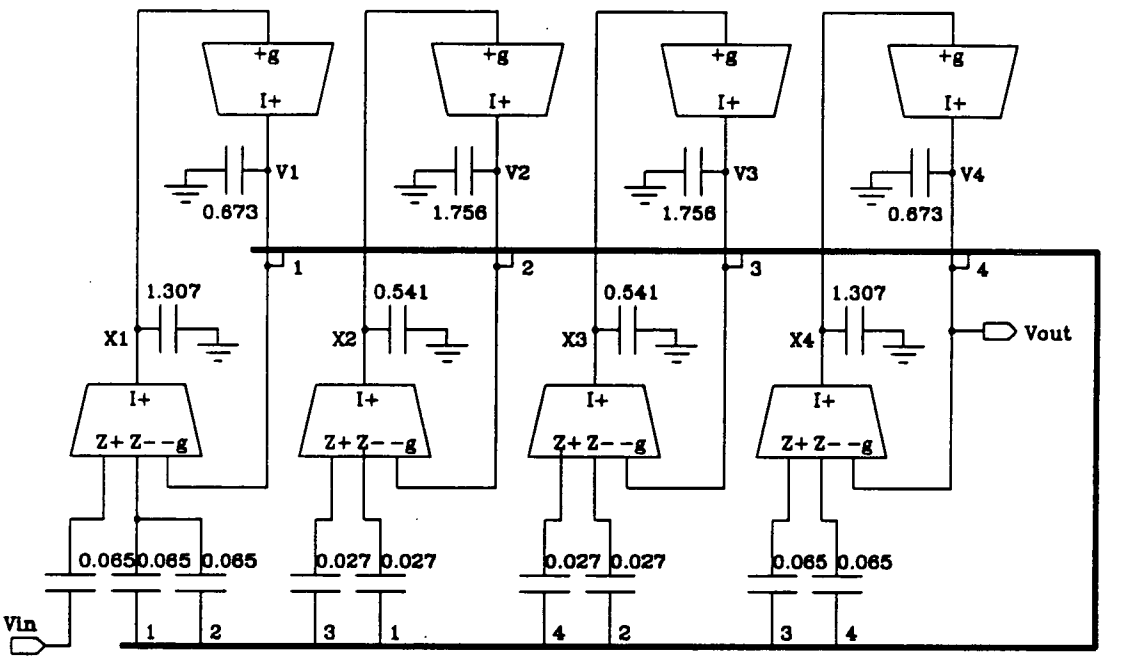


Figure 6.3-9 Eighth order Butterworth bandpass transconductor ladder, obtained using a VI representation and the LD decomposition

Before leaving this design example, it should be noted that an alternative VI representation of the eighth order all-pole prototype (figure 6.3-8) would be to construct **V** using V_1, V_2, V_3 and I_4. This representation has been recommended for obtaining canonical SC and active RC ladders of order 4n, however it is not suitable for transconductor ladder design by LD decomposition as the choice of V_2 instead of I_2 makes **C** and Γ non-diagonal.

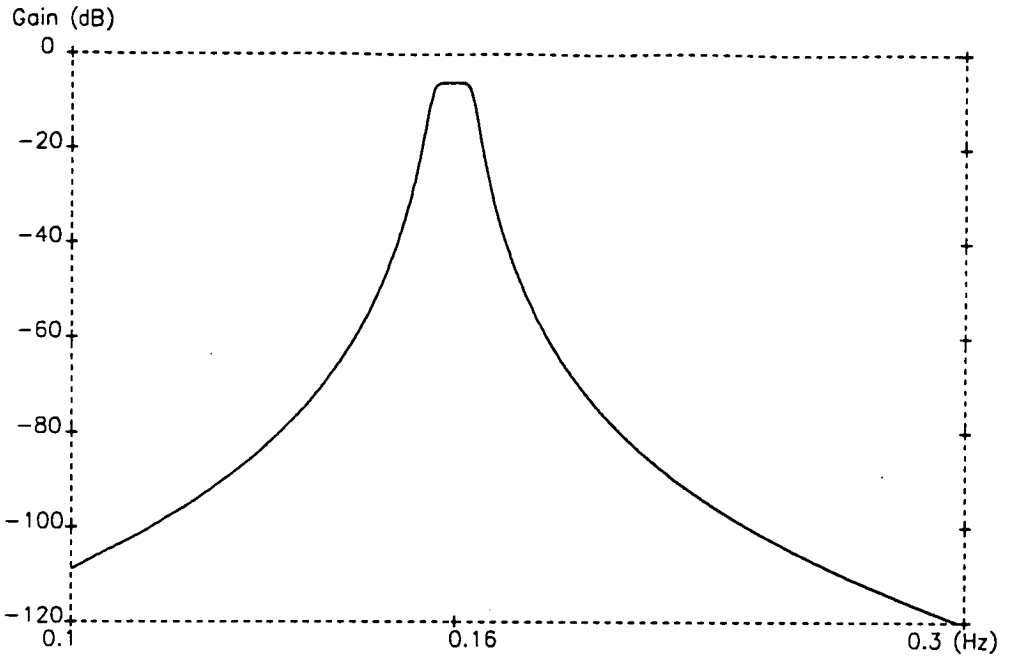


Figure 6.3-10 SPICE simulation of the eighth order Butterworth bandpass transconductor ladder shown in figure 6.3-9

In some cases it is not possible or desirable to use a transconductor with low impedance inputs as the building block for the active filter. The most obvious case is at higher frequencies (say >1MHz in CMOS), where a simpler transconductor is required to minimise the effects of excess phase. Fortunately, even when a conventional transconductor is to be used, there is a matrix decomposition available which gives active filter structures superior to conventional coupled biquad circuits.

*Right Inverse (RI) Decomposition**

We define the vector **X** of auxiliary voltage variables by

$$g\mathbf{X} = s^{-1}\Gamma\mathbf{V}, \tag{6.3-22}$$

where the scaling parameter g has the dimensions of conductance. Substituting 6.3-22 into 6.1-1 gives

$$\mathbf{J} = \mathbf{GV}+s\mathbf{CV}+g\mathbf{X} \tag{6.3-23}$$

---

*The application of the Right Inverse Decomposition to transconductor ladder design was suggested by Dr R.K. Henderson

The RI design equations are then found by rearranging 6.3-23 and multiplying 6.3-22 by Γ^{-1}:

$$\mathbf{CV} = s^{-1}[\mathbf{J}-\mathbf{GV}-g\mathbf{X}] \tag{6.3-24}$$

$$g\Gamma^{-1}\mathbf{X} = s^{-1}\mathbf{V}. \tag{6.3-25}$$

These equations can be implemented using conventional transconductors because there are no unidirectional non-integrated paths. All terms in the right hand side are integrated, and any non-integrated terms arising from the left hand side are bidirectional since $\mathbf{C}$ and Γ^{-1} are symmetric. It is possible (and likely in the majority of applications) for summing integrators to be required for (6.3-24), however three features of the RI decomposition make summing integrators acceptable in this case. Firstly, only two values of transconductance will be required: one for integrating $\mathbf{X}$ and $\mathbf{V}$, and the other for $\mathbf{J}$ and $\mathbf{GV}$. The absence of non-integer ratios in the summing integrators is due to the fact that the matrix Γ is prevented from premultiplying $\mathbf{V}$ in an integrated term by the inverse matrix operation. The only matrix premultiplying an integrated vector is $\mathbf{G}$, whose elements all have the same magnitude as long as the passive prototype has equal terminating resistors. Secondly, the ratio of the transconductances can always be given an integer value and the larger of the two constructed from unit transconductances in parallel (for matching accuracy). This is because the ratio is equal to the value of g, and whilst g must be chosen to scale the $\mathbf{X}$ and $\mathbf{V}$ peak values correctly, little dynamic range will be lost by rounding g to the nearest integer value. Thirdly, the smaller transconductance, which is likely to be more prone to inaccuracy, is used only in the input and termination branches which are the least sensitive parts of the ladder.

Whereas the VI representation of the passive prototype was found to be preferable for the left decompositions described above, the V representation is more suitable for the RI decomposition. This is because for any particular prototype the V representation gives a sparser $\mathbf{G}$ matrix which is desirable to minimise the number of instances of the smaller value of transconductance.

To illustrate the RI decomposition we shall obtain a transconductor ladder for the sixth order Chebyshev prototype which is shown in figure 6.3-5 and described by the matrices

$$\mathbf{J} = \begin{bmatrix} \frac{V_{in}}{R} \\ 0 \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, \qquad \mathbf{G} = \frac{1}{R}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} C_1+C_2 & -C_2 & 0 \\ -C_2 & C_3 & 0 \\ 0 & 0 & C_5 \end{bmatrix}, \quad \Gamma = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_3} & \frac{-1}{L_4} \\ 0 & \frac{-1}{L_4} & \frac{1}{L_4}+\frac{1}{L_5} \end{bmatrix}. \qquad \text{(6.3-26a-e)}$$

Substituting these matrices into 6.3-24 and 6.3-25, the RI design equations for the Chebyshev prototype can be written explicitly:

$$V_1 = \frac{1}{sC_{11}}[\alpha g V_{in} - \alpha g V_1 - g X_1 - sC_{12} V_2]$$

$$V_2 = \frac{1}{sC_{22}}[-g X_2 - sC_{21} V_1]$$

$$V_3 = \frac{1}{sC_{33}}[-g X_3 - \alpha g V_3]$$

$$X_1 = \frac{g}{s(g^2 L_{11})} V_1$$

$$X_2 = \frac{1}{s(g^2 L_{22})}[g V_2 - s(g^2 L_{23}) X_3]$$

$$X_3 = \frac{1}{s(g^2 L_{33})}[g V_3 - s(g^2 L_{32}) X_2]. \qquad \text{(6.3-27a-f)}$$

where as before C_{ij} and L_{ij} are the elements of $\mathbf{C}$ and Γ, and $\alpha = \frac{1}{gR}$. Each of these equations can be implemented using a first order section with a conventional transconductor (figure 5.3-1), to give the ladder shown in figure 6.3-11. Since Γ^{-1} is symmetric, the non-integrated term in 6.3-27a equals that in 6.3-27b. This, along with the fact that the transconductors have high impedance outputs, means that both terms can be realised using a single capacitor (two in the fully differential circuit). Such a capacitor gives a "bidirectional coupling path". The same consideration applies to the non-integrated terms in 6.3-27e and 6.3-27f.

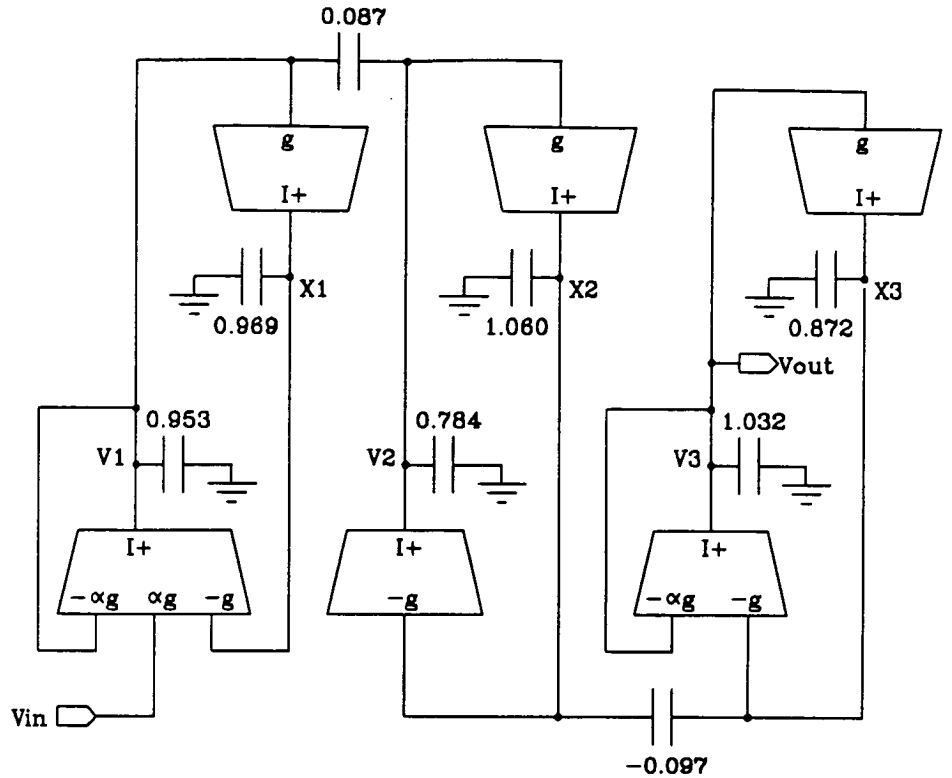


Figure 6.3-11 Sixth order Chebyshev bandpass ladder, obtained by Right Inverse decomposition

Now we discuss the design of bandpass ladders with finite transmission zeros. Symmetric bandpass prototypes can be obtained by transformation of lowpass ladders such as the third order elliptic ladder shown in figure 6.3-12. This figure is included because the way the lowpass ladder is transformed to bandpass affects the eventual active circuit significantly.

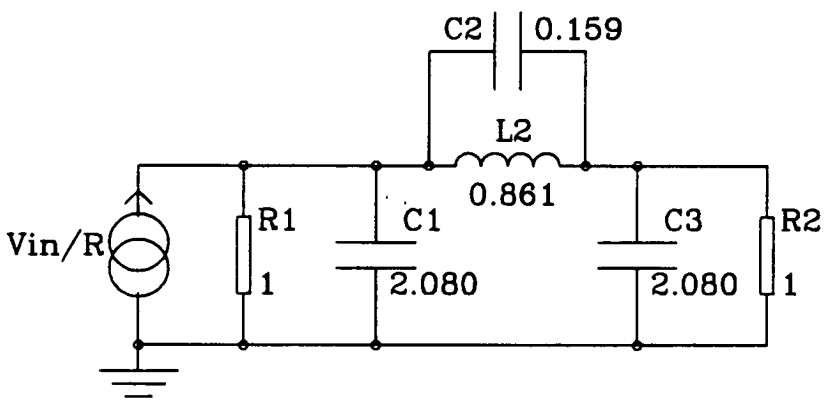


Figure 6.3-12 Lowpass elliptic ladder used for transformation to bandpass ladder

If the components L_2 and C_2 of figure 6.3-12 are transformed together [59], the sixth order elliptic bandpass ladder shown in figure 6.3-13 is obtained. L_2 and C_2 in the

lowpass ladder transform to two tank circuits in series, (L_2,C_2) and (L_4,C_4). The extra components, C_3 and L_3, are introduced by scaling the nodal voltage V_2 by the method described on page 127. The magnitude response of this ladder is shown in figure 6.3-14.

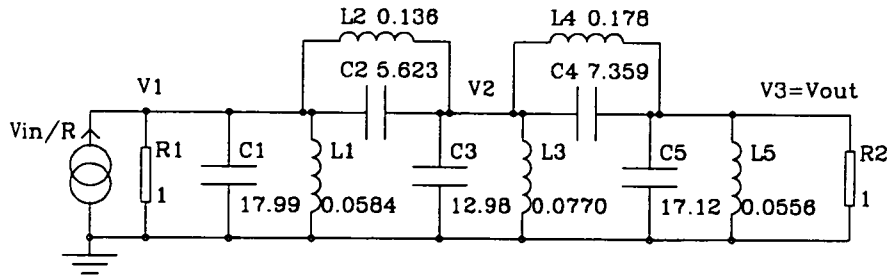


Figure 6.3-13 Sixth order elliptic bandpass prototype

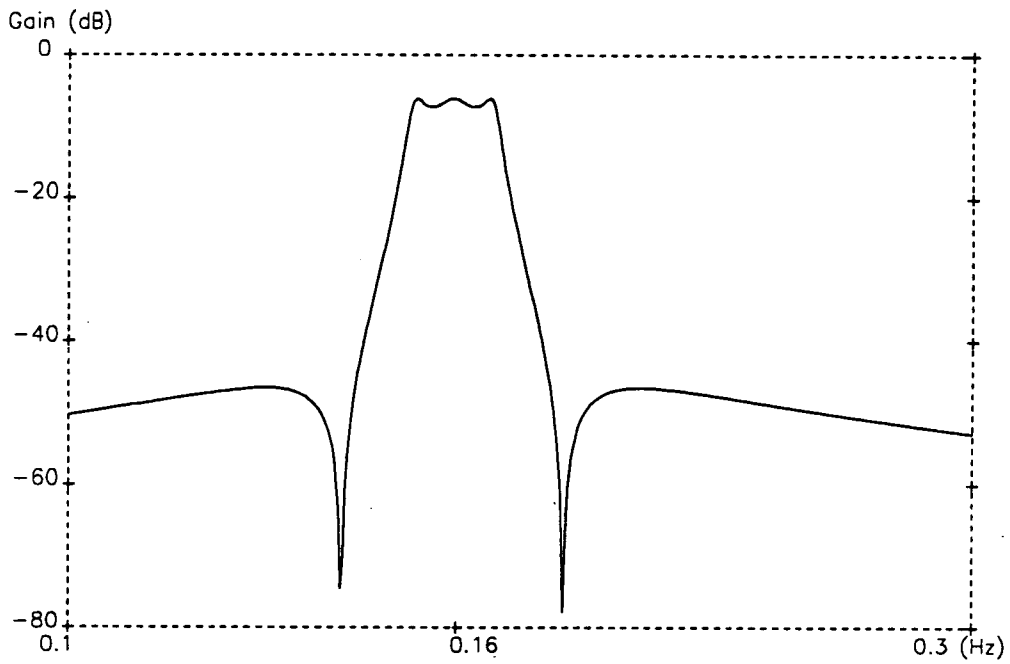


Figure 6.3-14 Magnitude response of sixth order elliptic bandpass prototype

Since this ladder is comprised only of *parallel* LC pairs, it is best to use the V representation, in which case it is described by the matrices

$$\mathbf{J} = \begin{bmatrix} \frac{V_{in}}{R} \\ 0 \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, \qquad \mathbf{G} = \frac{1}{R}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix},$$

$$C = \begin{bmatrix} C_1+C_2 & -C_2 & 0 \\ -C_2 & C_2+C_3+C_4 & -C_4 \\ 0 & -C_4 & C_5 \end{bmatrix},$$

and

$$\Gamma = \begin{bmatrix} \frac{1}{L_1} & \frac{-1}{L_2} & 0 \\ \frac{-1}{L_2} & \frac{1}{L_2}+\frac{1}{L_3}+\frac{1}{L_4} & \frac{-1}{L_4} \\ 0 & \frac{-1}{L_4} & \frac{1}{L_4}+\frac{1}{L_5} \end{bmatrix}. \qquad (6.3\text{-}28a\text{-}e)$$

Since Γ is not diagonal, the Left Direct decomposition cannot be used, so we try the Left Inverse (type 1). This gives the ladder shown in figure 6.3-15. The interconnect of this circuit is quite complex and the number of capacitors large, due to the fact that the inverse of the tridiagonal Γ is a full matrix. A full matrix gives a complexity which increases proportionately to the square of the filter order. For a sixth order filter this complexity is manageable, but it would not be so for higher orders.

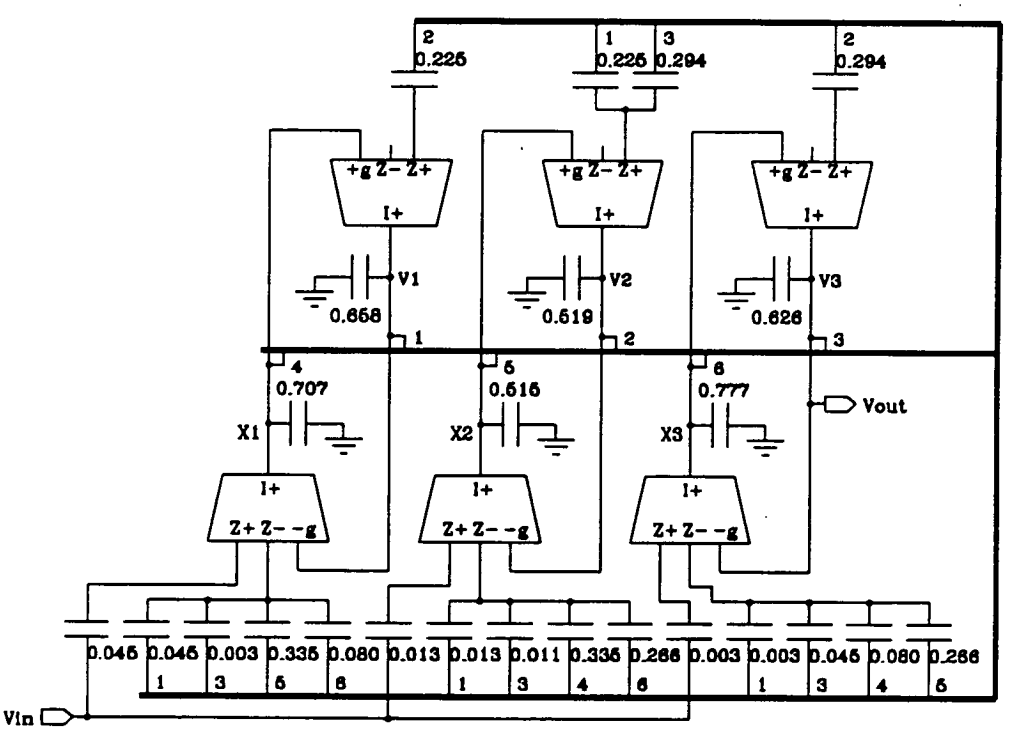


Figure 6.3-15 Sixth order elliptic bandpass ladder obtained using prototype of figure 6.3-13 and LI (type1) decomposition

Fortunately a simpler structure is obtained by using a different prototype and a different LI decomposition. First we give the decomposition, since the its design equations indicate the desired properties of the prototype.

Left Inverse Decomposition (Type 2)
In the general LI decomposition, defined by 6.3-14 and 6.3-15, let:

$$\mathbf{C}_l = \mathbf{C}$$

and

$$\mathbf{C}_r = \mathbf{I}. \qquad \text{(6.3-29a,b)}$$

From (6.3-12) it can then be seen that this gives σ the dimensions of angular frequency, and for clarity we rename the scaling factor

$$\sigma = \omega_o. \qquad \text{(6.3-30)}$$

Substituting (6.3-29) and (6.3-30) into (6.3-14) and (6.3-15) gives the design equations for the LI (type2) decomposition:

$$\omega_o \Gamma^{-1}\mathbf{C}\mathbf{X} = \Gamma^{-1}\mathbf{J} - \Gamma^{-1}\mathbf{G}\mathbf{V} - s^{-1}\mathbf{V} \qquad \text{(6.3-31)}$$

and

$$\mathbf{V} = \omega_o s^{-1}\mathbf{X}. \qquad \text{(6.3-32)}$$

The second of these equations is simple to implement because it contains no premultiplying matrices. The first equation will be greatly simplified if a prototype can be used for which $\Gamma=\mathbf{C}$, since the product premultiplying $\mathbf{X}$ then becomes the identity matrix. Unfortunately this condition is not met for the prototype shown in figure 6.3-15. However a suitable prototype can obtained by transforming each component of the lowpass prototype *individually* (instead of transforming L_2 and C_2 together as was done to obtain 6.3-13). For the third order lowpass elliptic ladder, this gives the sixth order bandpass prototype shown in figure 6.3-16.

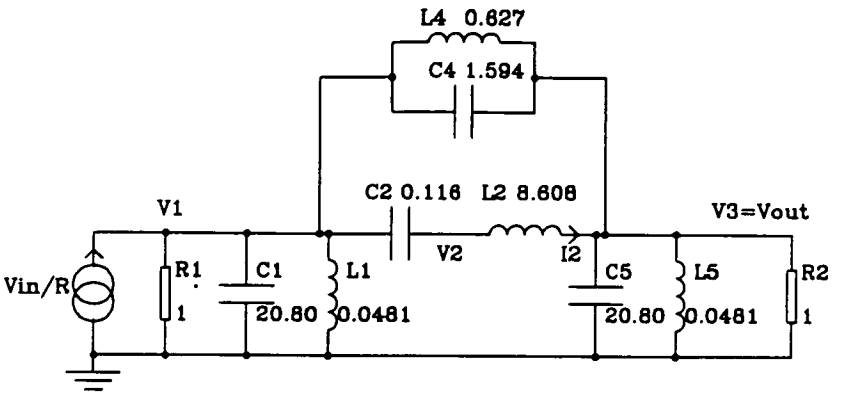


Figure 6.3-16 Sixth order elliptic bandpass RLC ladder, obtained by transformation of each component of the lowpass ladder individually

This ladder is described in the VI representation by the matrices

$$\mathbf{J} = \begin{bmatrix} \frac{V_{in}}{R} \\ 0 \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_{I2} \\ V_3 \end{bmatrix}, \qquad \mathbf{G} = \frac{1}{R}\begin{bmatrix} 1 & 1 & 0 \\ 1 & 0 & -1 \\ 0 & -1 & 1 \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} C_1+C_4 & 0 & -C_4 \\ 0 & \frac{-L_2}{R^2} & 0 \\ -C_4 & 0 & C_3+C_4 \end{bmatrix},$$

and

$$\Gamma = \begin{bmatrix} \frac{1}{L_1}+\frac{1}{L_4} & 0 & \frac{-1}{L_4} \\ 0 & \frac{-1}{C_2R^2} & 0 \\ \frac{-1}{L_4} & 0 & \frac{1}{L_3}+\frac{1}{L_4} \end{bmatrix}. \qquad \text{(6.3-33a-e)}$$

Since each component of the lowpass prototype was transformed individually and the bandpass ladder is normalised to a centre frequency of 1rad/sec and a termination resistance of 1 ohm, the transformation equations [4,59] imply that:

$$C_i = \frac{1}{L_i}. \qquad \text{(6.3-34)}$$

Therefore $\mathbf{C} = \Gamma$ and the LI (type 2) design equations reduce to

$$\omega_0 \mathbf{X} = \Gamma^{-1}\mathbf{J} - \Gamma^{-1}\mathbf{G}\mathbf{V} - s^{-1}\mathbf{V} \tag{6.3-35}$$

and

$$\mathbf{V} = \omega_0 s^{-1}\mathbf{X}. \tag{6.3-36}$$

For the matrices (6.3-33a-f) these equations give the transconductor ladder shown in figure 6.3-17. This ladder compares favourably (in terms of number of capacitors and complexity of interconnect) with that obtained using the V representation and the LI (type 1) decomposition (figure 6.3-15).

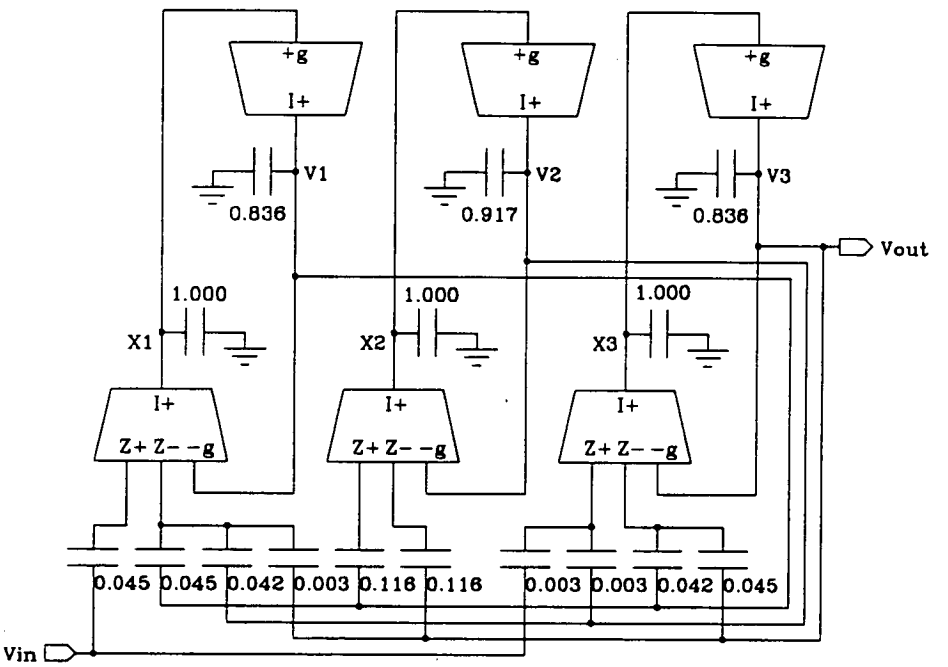


Figure 6.3-17 Sixth order elliptic bandpass transconductor ladder, obtained from prototype of figure 6.3-16 by VI representation and LI (type2) decomposition

Using the VI representation and the Left Inverse (type 2) decomposition, even higher order symmetric responses with transmission zeroes can be realised without the excessive circuit complexity that would seem to follow inevitably from the matrix inversion. Figures 6.3-18 to 6.3-20 show the prototype, transconductor ladder and simulated response for a tenth order elliptic bandpass filter.

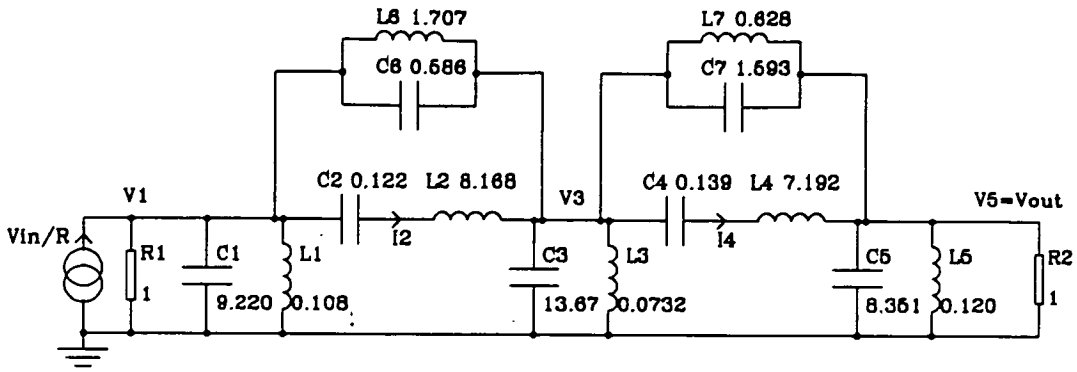


Figure 6.3-18 Passive prototype for tenth order elliptic bandpass ladder

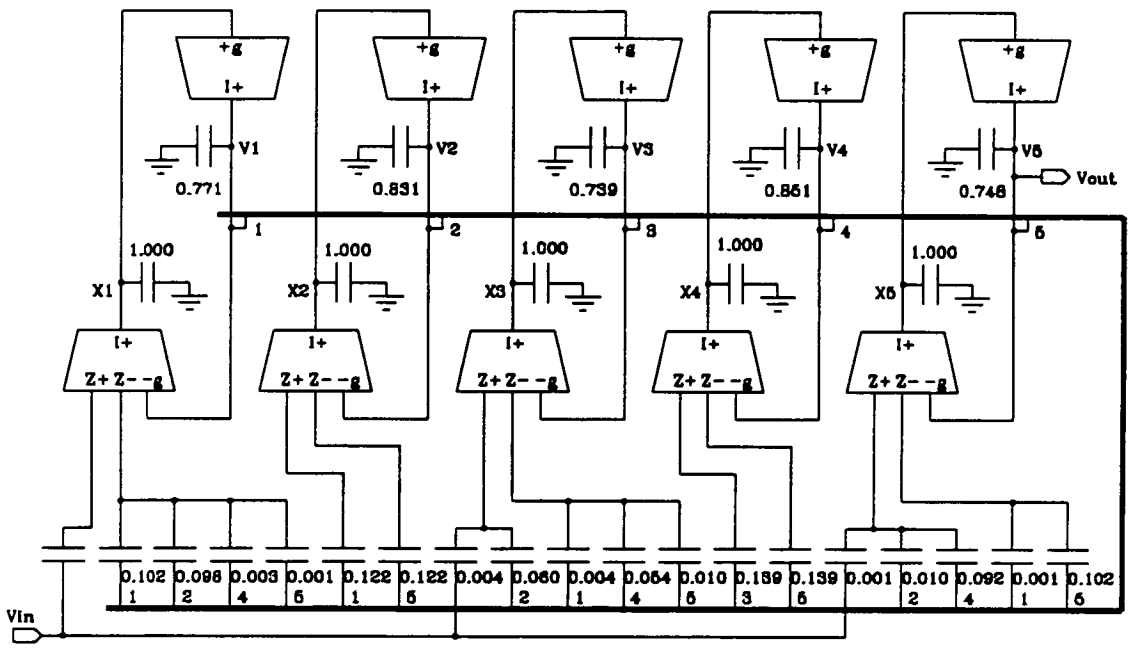


Figure 6.3-19 Tenth order elliptic bandpass transconductor ladder

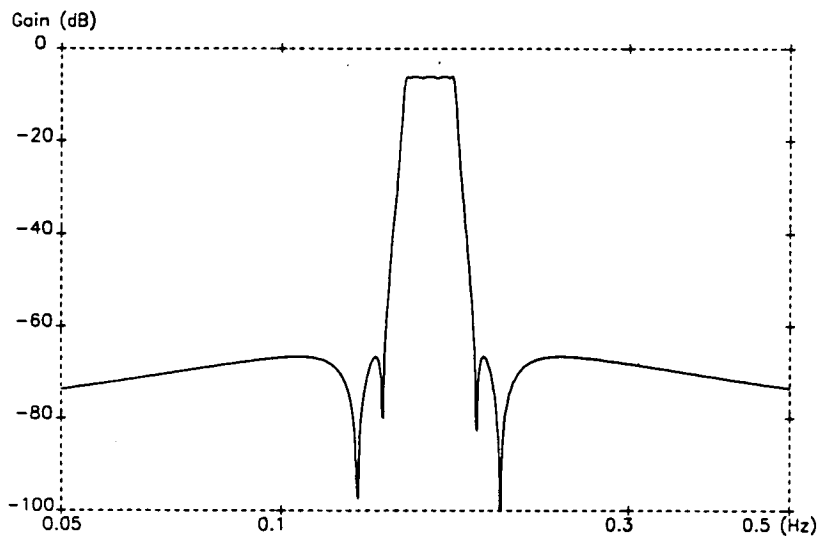


Figure 6.3-20 Simulation of tenth order elliptic bandpass transconductor ladder

As in the case of all-pole bandpass filters, the Right Inverse decomposition gives the best results if transconductors with low impedance inputs are not to be used. Figure 6.3-21 shows the RI transconductor ladder obtained from the prototype of figure 6.3-13.

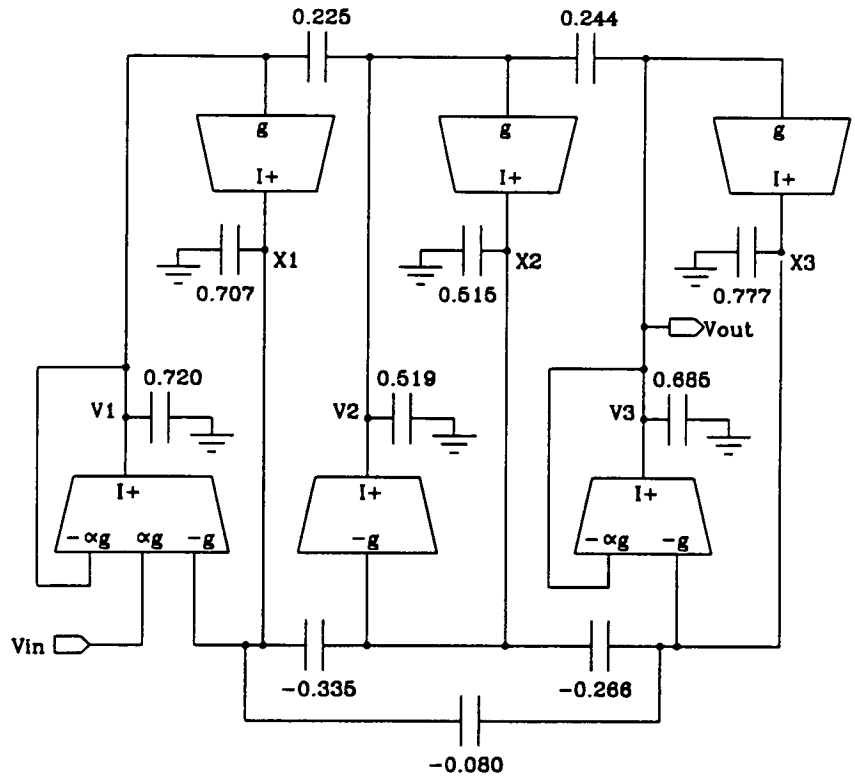


Figure 6.3-21 Sixth order elliptic bandpass ladder, obtained using V representation of figure 6.3-13, and RI decomposition

An alternative way to maintain a simple structure for higher order filter containing transmission zeros is to use a prototype and representation giving a Γ matrix which preserves its sparsity upon inversion. This precludes an elliptic response, however in practical applications it is not uncommon for a bandpass filter to require a much sharper attenuation in one stopband than the other. In such a case it may suffice to use an asymmetric response which has zeros in only one stopband. The omission of the corresponding zeros in the other stopband can greatly simplify the Γ matrix and its inverse.

Asymmetric passive and transconductor ladders represent an interesting line of further research. Here we merely make the observation that prototypes whose Γ matrices are block diagonal would be suitable since block diagonal matrices experience no loss of sparsity upon inversion [75]. Such prototypes contain two or more groups of nodes which are connected to each other only by capacitors.

6.4 Highpass ladders

As in the case of bandpass ladders, we will first examine the realisation of all-pole responses and then responses with finite transmission zeros. In the design of highpass ladders some of the decompositions defined in the previous sections will be reapplied, and one new decomposition will be introduced.

Figure 6.4-1 shows a third order all-pole RLC prototype obtained by transformation of a lowpass ladder. The component values shown are for a Chebyshev response with 0.01dB passband ripple. The first observation is that we cannot obtain a *canonical* active realisation. This is because we have to simulate the two nodal voltages, since the termination resistors are not in series with any other components, and an auxiliary variable will be required to simulate the behaviour of each of the grounded inductors. Therefore we look for an efficient fourth order active realisation.

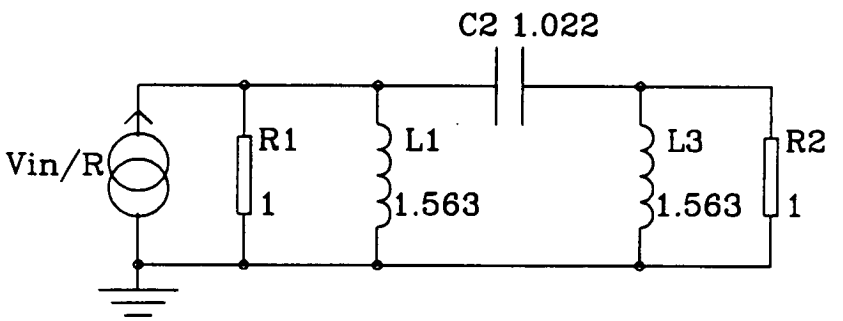


Figure 6.4-1 Third order all-pole highpass RLC ladder

The third order all-pole prototype is described in the V representation by the matrices:

$$\mathbf{J} = \begin{bmatrix} \frac{V_{in}}{R} \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_3 \end{bmatrix}, \qquad \mathbf{G} = \frac{1}{R}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} C_2 & -C_2 \\ -C_2 & C_2 \end{bmatrix}, \quad \text{and} \quad \Gamma = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_3} \end{bmatrix}. \qquad \text{(6.4-1a-e)}$$

The simplest matrix method to obtain the active circuit for this prototype is the Right Direct (RD) decomposition:

Right Direct Decomposition

The auxiliary variable vector **X** is defined by the first design equation:

$$g\mathbf{X} = s^{-1}\Gamma\mathbf{V} \tag{6.4-2}$$

The second design equation is obtained by substituting (6.4-2) into (6.1-1) and rearranging:

$$\mathbf{CV} = s^{-1}[\mathbf{J}-\mathbf{GV}-g\mathbf{X}] \tag{6.4-3]}$$

The principal features of the RD decomposition can be observed from (6.4-2) and (6.4-3). Firstly, conventional transconductors can be used because the only non-integrated terms are the bidirectional paths arising from the symmetric matrix **C** premultiplying **V** in (6.4-3). Secondly, two values of transconductance in integer ratio may be required to realise (6.4-3) if the scaling parameter g takes a non-unity value. Thirdly, acceptable ratios of transconductance will occur in the filter *only* if Γ is diagonal or if the coefficients on each row are in simple integer ratio. This restriction on the form of Γ makes the RD decomposition unsuitable for use in symmetric *bandpass* filters (in fact it would give "coupled biquad" bandpass ladders, the problems of which were demonstrated in chapter 3). However for all-pole highpass ladders Γ is diagonal and the RD decomposition can be used.

For the matrices (6.4-2) the rows of the RD design equations can be written explicitly:

$$V_1 = \frac{g}{sC_2}[\alpha V_{in}-\alpha V_1-X_1-sC_2V_2]$$

$$V_2 = \frac{g}{sC_2}[-\alpha V_2-X_2-sC_2V_1]$$

$$X_1 = \frac{g}{sC_{L1}}V_1$$

$$X_2 = \frac{g}{sC_{L2}}V_2 \tag{6.4-4a-d}$$

with

$$C_{Li} = g^2 L_i. \tag{6.4-5}$$

and

$$\alpha = \frac{1}{gR} \tag{6.4-6}$$

Implementing each of (6.4-4a-d) with a conventional transconductor first order section (figure 5.3-1) gives the ladder a single ended version of which shown in figure 6.4-2. The optimum value of α was chosen by simulating the ladder with different values. Figure 6.4-3 shows the result of the SPICE simulation of the fully differential circuit for g=1S and α=1.

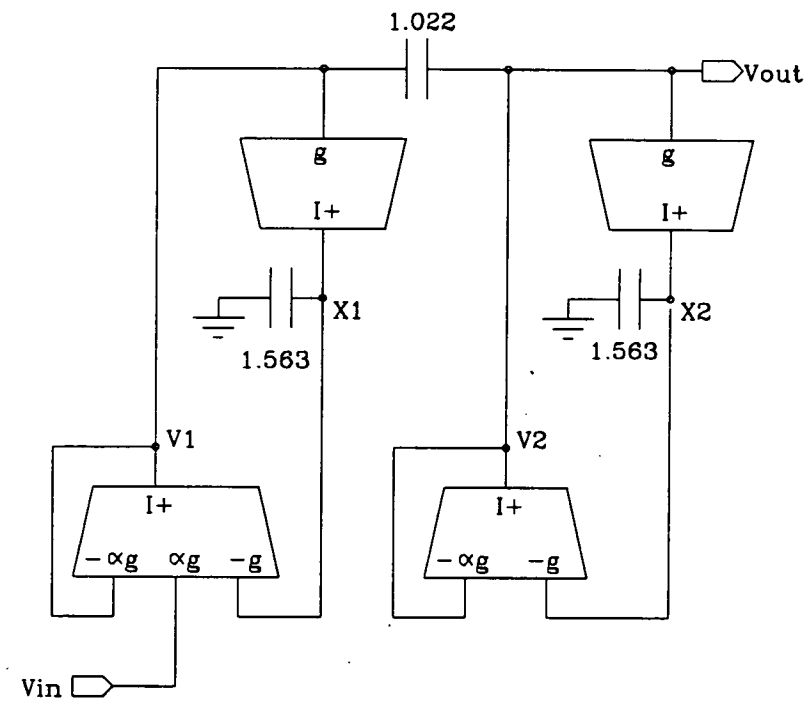


Figure 6.4-2 Third order highpass all-pole transconductor ladder, obtained by Right Direct decomposition

To realise the third order highpass all-pole ladder using transconductors with low impedance inputs and a single value of transconductance, either Left Direct or Left Inverse decompositions can be used since Γ is diagonal.

Now let us consider a third order elliptic highpass prototype, figure 6.4-4, whose amplitude response is shown in figure 6.4-5.

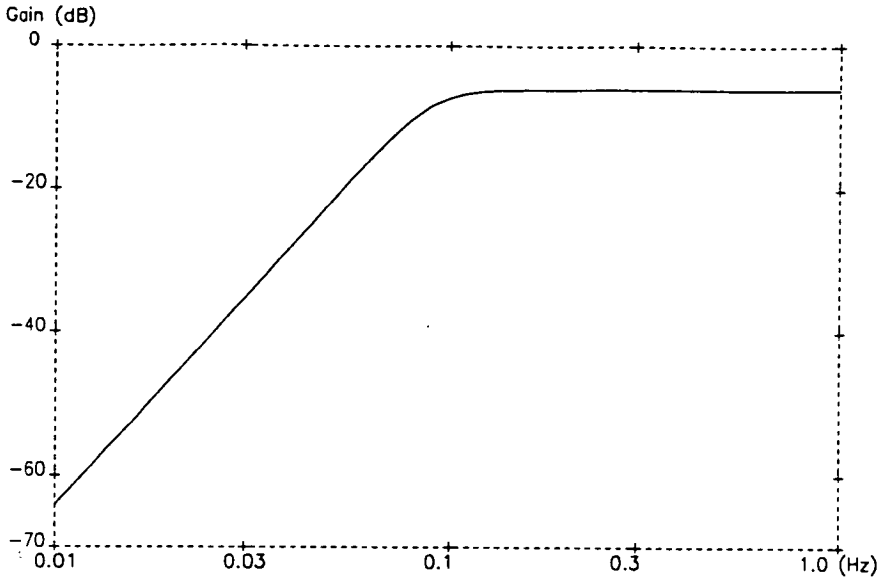


Figure 6.4-3 SPICE simulation of third order all-pole highpass transconductor ladder

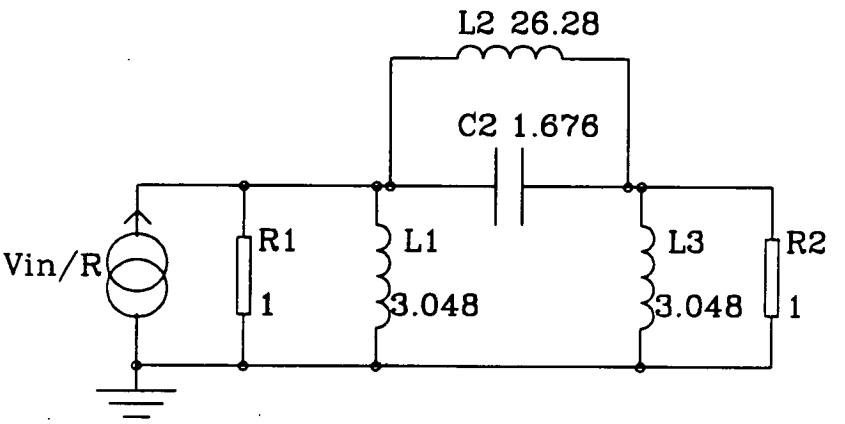


Figure 6.4-4 Third order elliptic RLC ladder

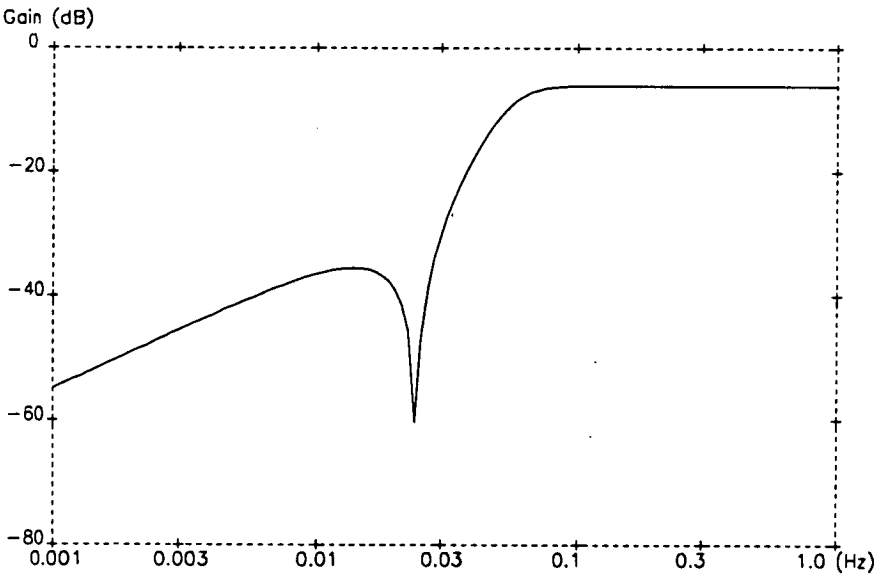


Figure 6.4-5 Magnitude response of third order elliptic highpass RLC ladder

The elliptic prototype is described in the V representation by the matrices:

$$\mathbf{J} = \begin{bmatrix} \frac{V_{in}}{R} \\ 0 \end{bmatrix}, \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \qquad \mathbf{G} = \frac{1}{R}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} C_2 & -C_2 \\ -C_2 & C_2 \end{bmatrix}, \quad \text{and} \quad \Gamma = \begin{bmatrix} \frac{1}{L_1}+\frac{1}{L_2} & \frac{-1}{L_2} \\ \frac{-1}{L_2} & \frac{1}{L_2}+\frac{1}{L_3} \end{bmatrix}. \qquad (6.4\text{-}7a\text{-}e)$$

In this case a simulation of the inductors using gyrators would give a fifth order ladder, and the RD decomposition would give a fourth order ladder with unpleasant transconductor ratios since Γ is not diagonal. Fortunately the RI decomposition can be used to give an elegant fourth order active ladder with only two values of transconductance. For the prototype of figure 6.4-4 a single ended version of the RI transconductor ladder is shown in figure 6.4-6.

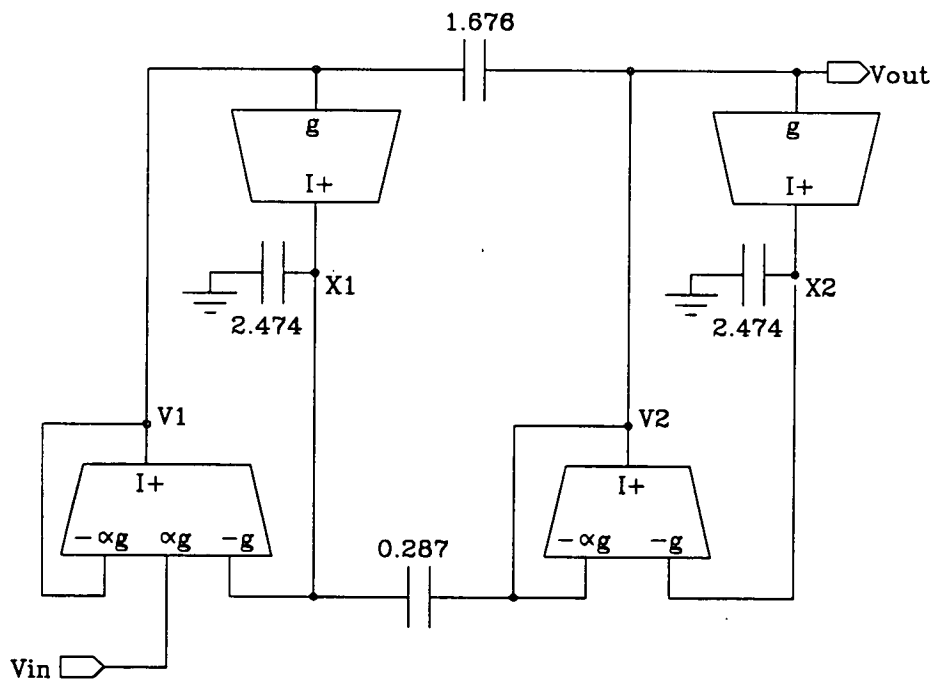


Figure 6.4-7 Right Inverse third order highpass elliptic transconductor ladder (single ended version)

To realise the highpass elliptic ladder using transconductors with low impedance inputs, the Left Inverse decomposition is again required due to the non-diagonal Γ matrix.

6.5 Bandstop ladders

Bandstop are the most problematical type to design, whether using conventional or matrix methods. As in the case of highpass ladders, canonical realisations cannot be attained. However an additional problem is that since a bandstop filter has finite transmission at d.c., we cannot use any left decomposition (all of which require capacitive input branches). The method presented here is applicable only to filters derived from all-pole lowpass prototypes. A decomposition has yet to be found for elliptic bandstop filters that does not give a transconductor ladder with much higher order than the prototype

Figure 6.5-1 shows a sixth order bandstop RLC ladder obtained by frequency transformation of a third order Butterworth lowpass ladder.

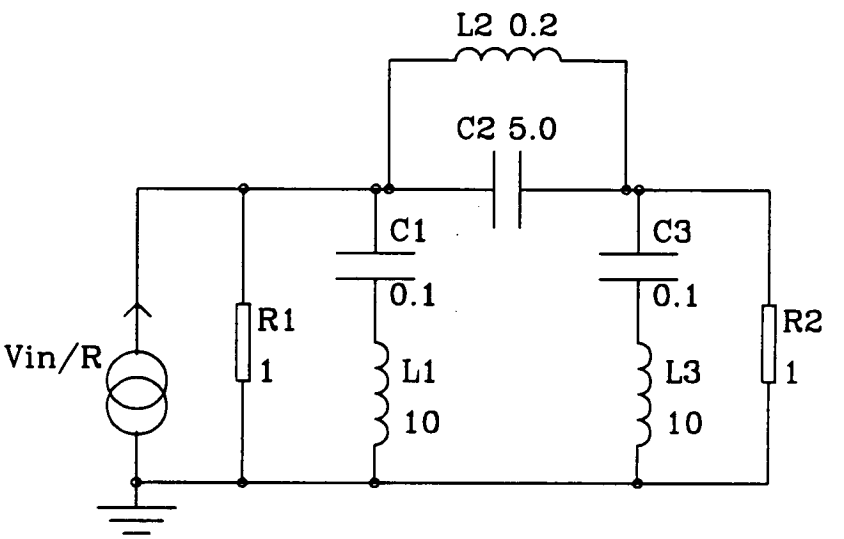


Figure 6.5-1 Sixth order Butterworth bandstop RLC ladder

The V representation is not very suitable for this ladder, because as figure 6.5-2 shows, the voltages on nodes 2 and 4 have peak values well above that of the output. This peaking becomes greater as the stopband is made more narrow. Applying the scaling technique introduced in section 6.3 produces matrices which can no longer be interpreted as a real passive ladder, in the sense that nodes occur whose total capacitive load is less than the total load of coupling capacitance. Such matrices can be realised as an active circuit only if first order sections are available which have low impedance input *and* output. Therefore the V representation can be used to design bandstop filters only if closed loop integrators (chapter1) are used.

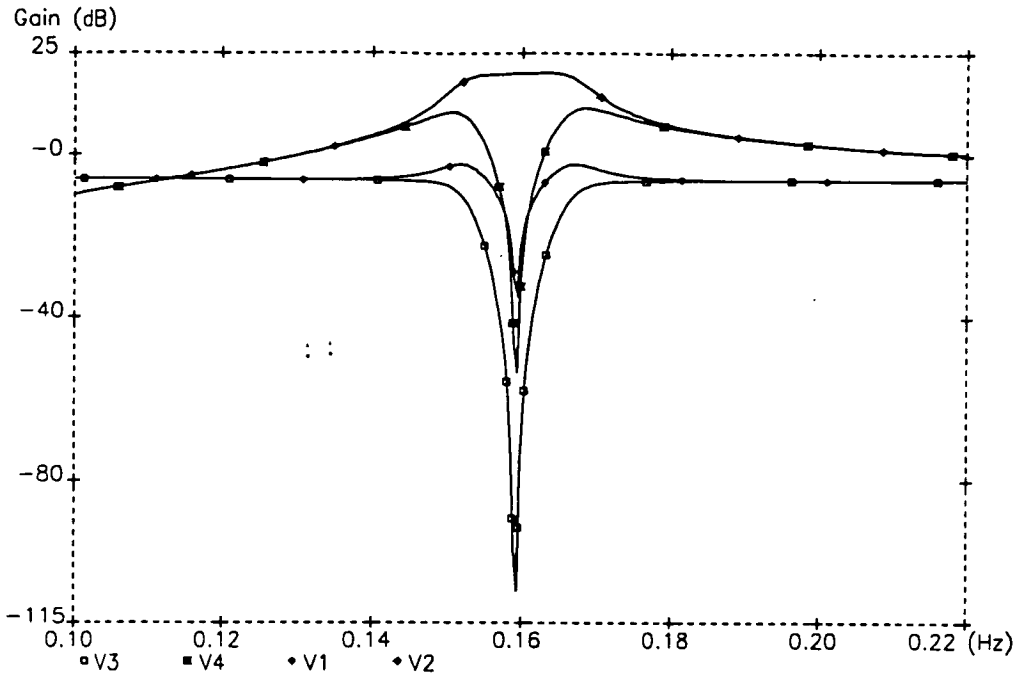


Figure 6.5-2 Nodal voltages of sixth order Butterworth bandstop ladder

Fortunately this restriction does not exist with the VI representation. Figure 6.5-3 show the variables of the prototype used to form the V vector in this case. These variables all have peak values within a few dB of each other.

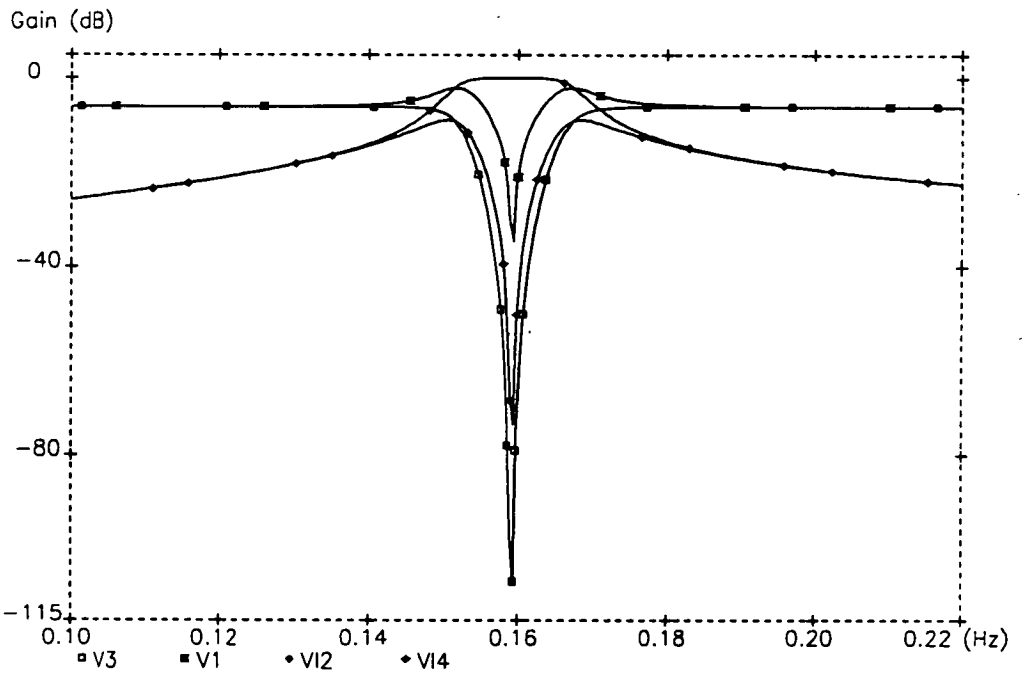


Figure 6.5-3

Variables of sixth order Butterworth bandstop ladder used in VI representation

The ladder of figure 6.5-1 is described in the VI representation by the matrices:

$$\mathbf{J} = \begin{pmatrix} \frac{V_{in}}{R} \\ 0 \\ 0 \\ 0 \end{pmatrix}, \qquad \mathbf{V} = \begin{pmatrix} V_1 \\ V_{I2} \\ V_3 \\ V_{I4} \end{pmatrix}, \qquad \mathbf{G} = \frac{1}{R}\begin{pmatrix} 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix},$$

$$\mathbf{C} = \begin{pmatrix} C_2 & 0 & -C_2 & 0 \\ 0 & \frac{-L_2}{R^2} & 0 & 0 \\ -C_2 & 0 & C_2 & 0 \\ 0 & 0 & 0 & \frac{-L_3}{R^2} \end{pmatrix}, \qquad \Gamma = \begin{pmatrix} \frac{1}{L_2} & 0 & \frac{-1}{L_2} & 0 \\ 0 & \frac{-1}{R^2C_1} & 0 & 0 \\ \frac{-1}{L_2} & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 & \frac{-1}{R^2C_3} \end{pmatrix}. \qquad (6.5\text{-}1a\text{-}e)$$

The Γ matrix defined by 6.5-1e has two unusual features. Firstly, its determinant has zero value, so Γ^{-1} is singular and hence an inverse decomposition cannot be used. Secondly, on the rows of Γ which have more than one non-zero element, these elements have the same magnitude. This permits the Right Direct decomposition to be applied in spite of the fact that Γ is not diagonal. The RD Butterworth bandstop transconductor ladder is shown in figure 6.5-4. This is a seventh order active circuit realising a sixth order transfer function.

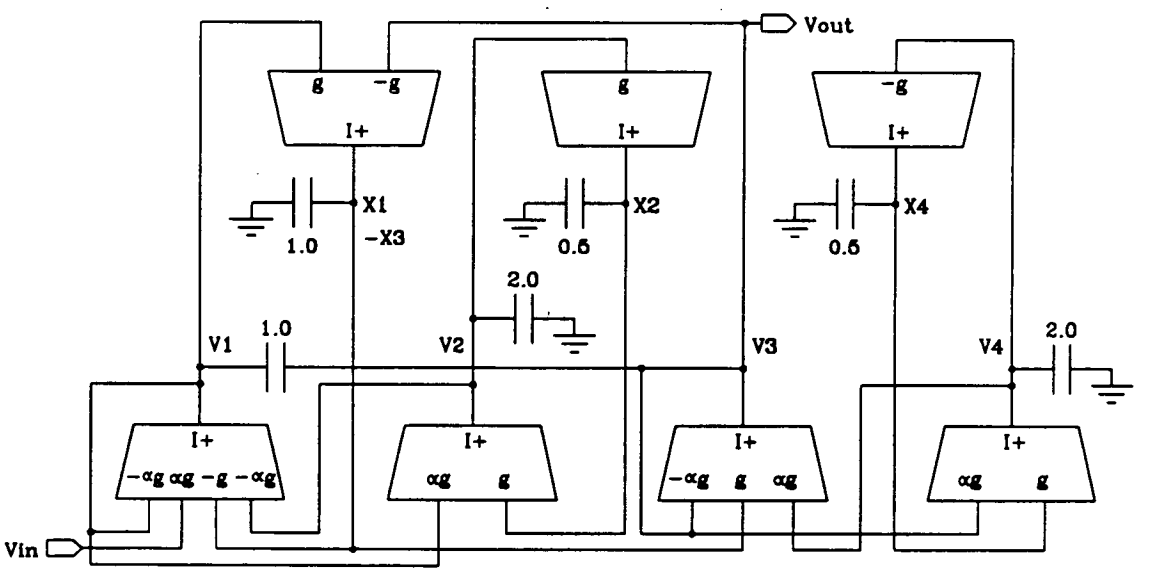


Figure 6.5-4 Sixth order Butterworth bandstop transconductor ladder, obtained using VI representation and RD decomposition (g=1, α=0.2)

6.6 Allpass ladders

Allpass filters are used to provide equalisation for the group delay distortion that occurs in recursive amplitude response filters. Group delay is the derivative of the phase shift through a filter with respect to frequency. In a filter with a linear phase response (such as a digital finite impulse response filter) the group delay is constant. However most analogue filters (including all those described so far in this thesis) have a non-linear phase response giving a frequency dependent group delay.

Usually group delay equalisation is provided in analogue filters by one or more allpass biquadratic stages [4]. However where the equaliser needs an order of greater than two it would be preferable to use a ladder, for the usual reasons of sensitivity to component value variations. In this section we demonstrate that a method for allpass transconductor ladder design, directly analogous to techniques recently proposed for digital [69] and switched capacitor [70] filters can be applied easily to transconductor ladders.

We consider allpass transfer functions of the form

$$H(s) = k\frac{P(-s)}{P(s)}, \tag{6.6-1}$$

where P(s) is a Hurwitz polynomial of order n and k = 1 if n is odd order and k = -1 if n is even. The polynomial P(s) is separated into odd and even parts:

$$P(s) = E(s) + O(s). \tag{6.6-2}$$

We define

$$Y(s) = \begin{cases} \dfrac{E(s)}{O(s)} & \text{if n is even} \\ \dfrac{O(s)}{E(s)} & \text{if n is odd} \end{cases} \tag{6.6-3}$$

Substituting (6.6-2) and (6.6-3) into (6.6-1) gives

$$H(s) = \frac{1-Y(s)}{1+Y(s)} = \frac{2}{1+Y(s)} - 1 \tag{6.6-4}$$

Since P(s) is Hurwitz, Y(s) can be expanded as a continued fraction, and equation (6.4-4) can then be realised as the combination of a singly terminated RLC ladder and an active summing stage as shown in figure 6.6-1.

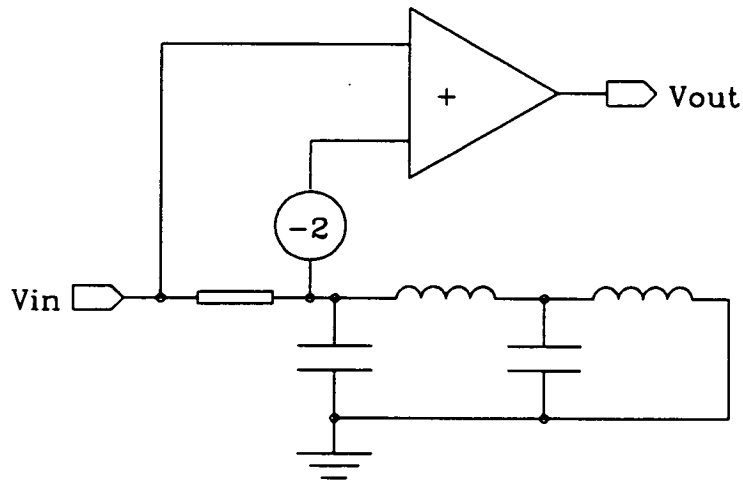


Figure 6.6-1 Prototype of an allpass ladder filter

Both the singly terminated ladder and the summer are implemented easily with a transconductor-capacitor circuit as shown in figure 6.6-2.

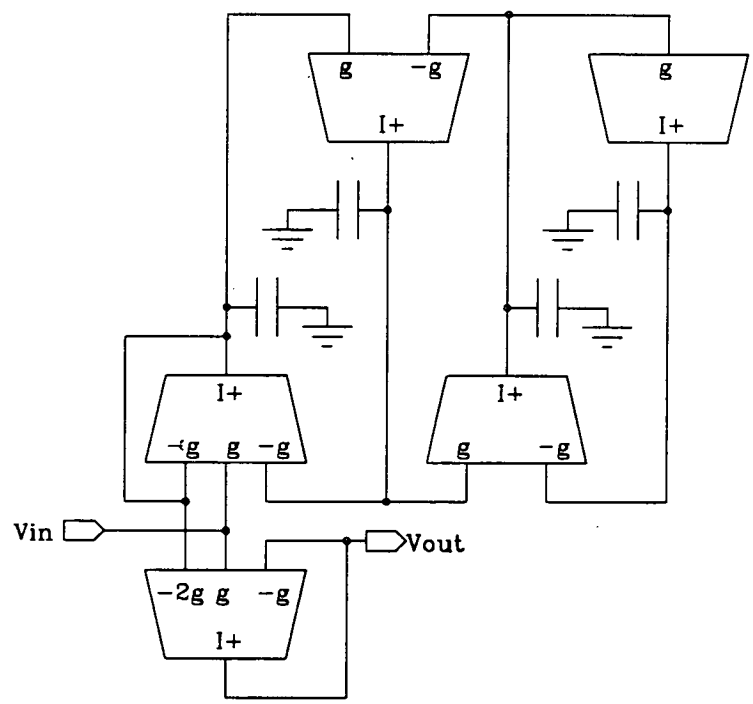


Figure 6.6-2 Allpass transconductor ladder filter

An example of a ladder equaliser is given in reference 65, a copy of which is bound with this thesis.

CHAPTER 7
EXPERIMENTAL FILTERS

7.1 Introduction

A set of filters and a frequency control loop have been designed and fabricated, in order to evaluate the circuits and design theory presented in this thesis. These have been included on two test chips produced on a 1μ double poly double metal CMOS process . Photomicrographs of the chips are shown in figure 7.1-1.

In this chapter we describe the performance of seven filters, the frequency control loop, and the buffer amplifier used to drive the filter output signals off chip. The filters have been designed using both conventional methods (chapter 3) and matrix methods (chapter 6). All of the filters use transconductors based on the novel "grounded quad" cell (chapters 4 and 5).

In the next section the methods and equipment used to evaluate the chips are described. In the remaining four sections of the chapter detailed results are given for the lowpass filters, the bandpass filters, the control loop and the output buffer respectively.

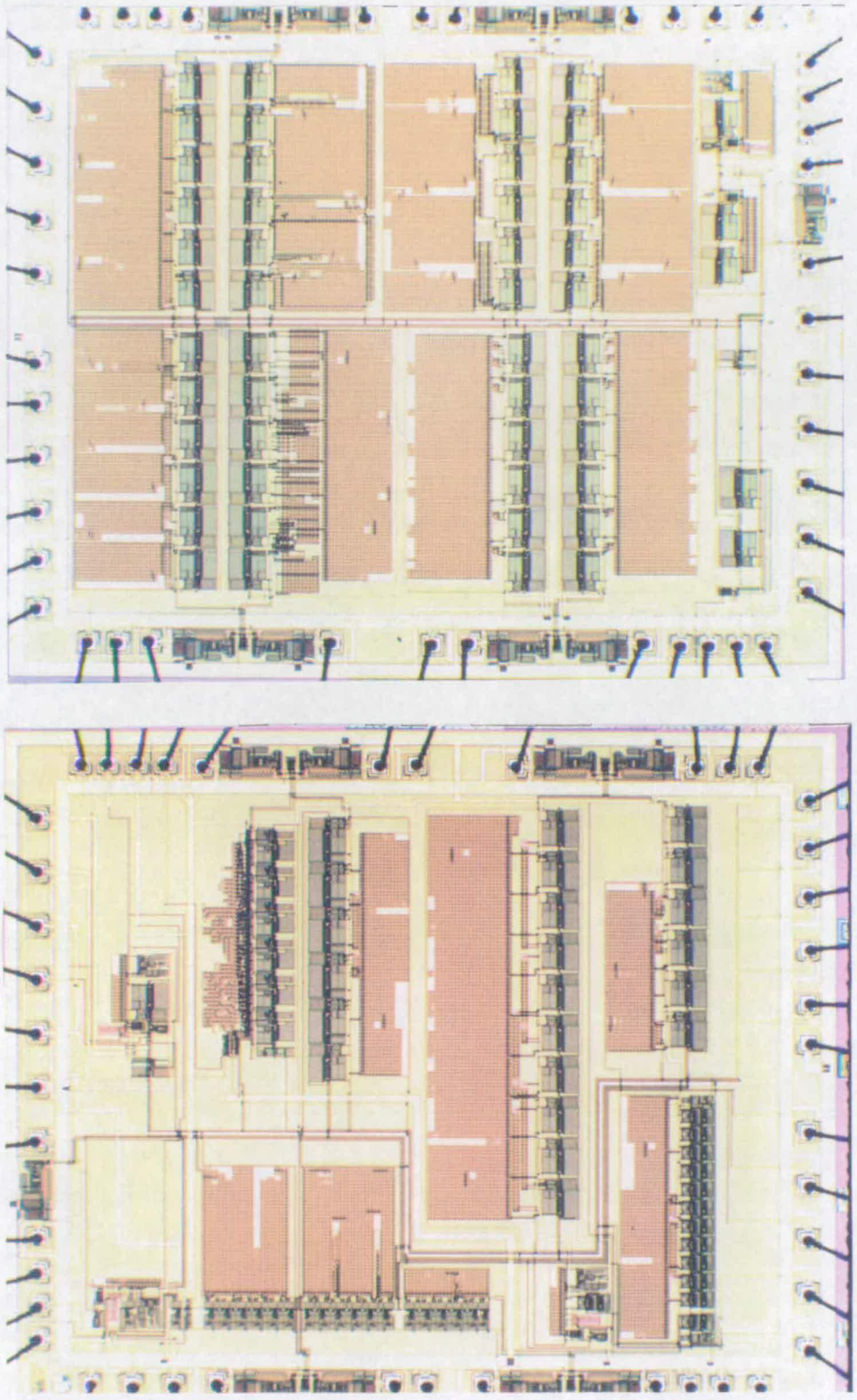


Figure 7.1-1 Photomicrographs of the two test chips

7.2 Evaluation methods

Each of the two test chips contains a number of different circuits. It is desirable that when one of these circuits is under test, all of the others should be disabled in order to allow the current consumption of the circuit under test (CUT) to be measured and to prevent signals being impaired by cross-talk. For this reason, at least one bias port of each circuit is brought off chip so that it can be connected to either the correct bias voltage (also pinned out) or the appropriate disabling power supply. The process of switching between filters is simplified by using analogue multiplexers to route the bias voltages. The multiplexers are controlled by a PC using a test program written in National Instruments' "Lab Windows" environment. The Lab Windows program is also used to control the nature of the signals (differential, single ended or common mode) applied to and received from the CUT. The complete evaluation arrangement for a filter and a control loop is illustrated in figure 7.2-1. There is a separate test board and control program for each of the two chips, however they are identical except for the arrangements of the multiplexers which are determined by the different pinouts.

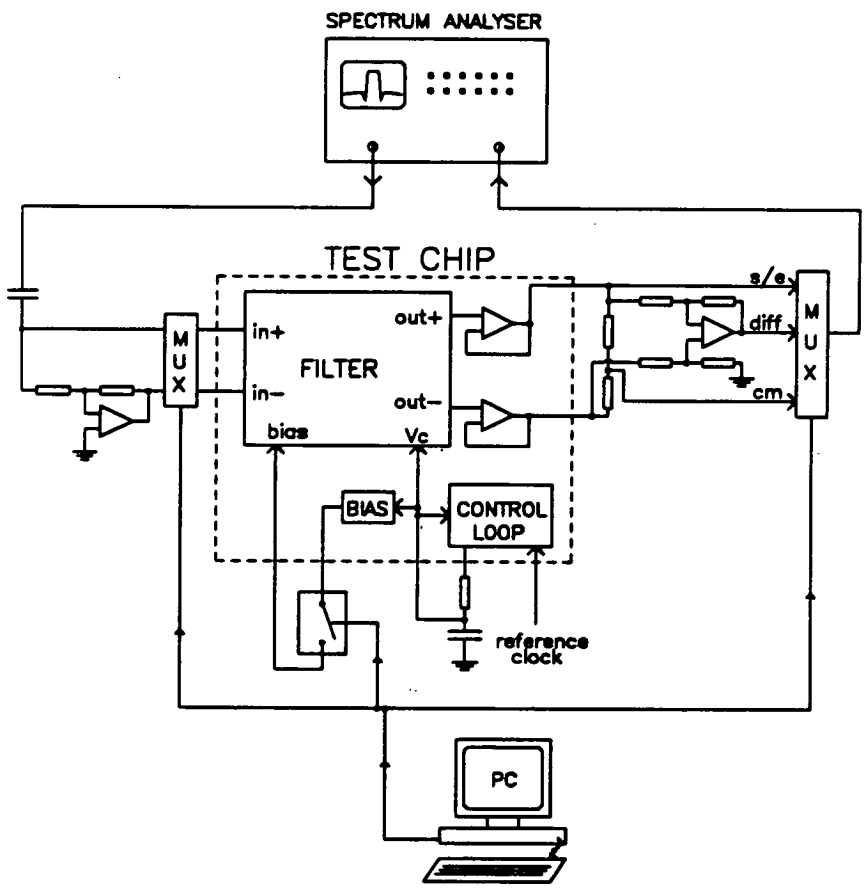


Figure 7.2-1 Evaluation arrangement for a selected filter and control loop

In this section some notes are given on the methods used to obtain each filter parameter. Also, we present evaluation results for one of the test boards alone (with the filter being replaced by two pieces of wire). These measurements have been taken to ensure that the results given in the following sections truly represent the performance of the CUTs and are not limited by that of the test board.

Amplitude response

This is measured using a spectrum analyser (Hewlett Packard HP3585A) to provide the sweeping source and analyse the filter output. The amplitude responses shown in this chapter were obtained by performing a screen dump from the spectrum analyser's display. The response of the test board alone is shown in figure 7.2-2. It is flat to within 0.1dB across a bandwidth from 10kHz to 1MHz.

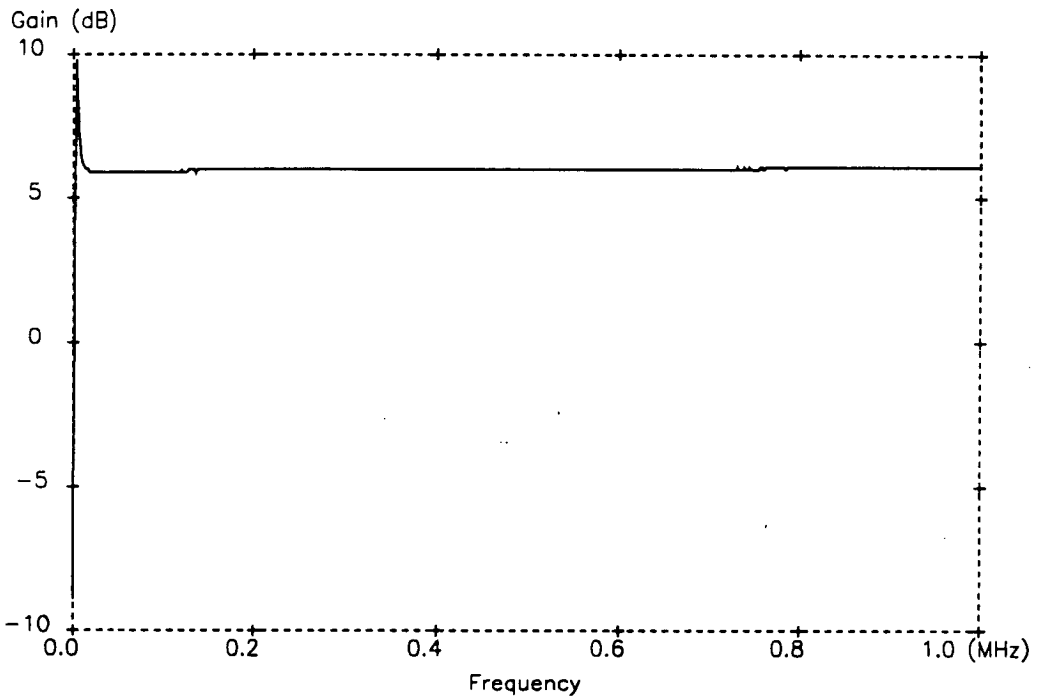


Figure 7.2-2 Amplitude response of test board

Noise

Noise spectra are obtained using the spectrum analyser as for amplitude responses, but with the input of the CUT grounded. It should be noted that these plots give noise *amplitude* (in dBm) rather than spectral density and they are therefore dependent upon the resolution bandwidth (rbw) setting on the analyser. Unless otherwise stated,

the rbw is set to 300Hz in each case. Noise spectral density (NSD) can also be found at specified frequencies using an option on the spectrum analyser. The NSD of the test board is approximately 60nV/$\sqrt{\text{Hz}}$ at 400kHz and 1MHz.

Total harmonic distortion (THD)

A sine wave at a fixed frequency is applied using a programmable oscillator (Tektronix SG5010) and the levels of the signal (a_1) and its harmonics (a_2, a_3, ...) in the CUT output are measured using the spectrum analyser. The THD figure is calculated using the formula

$$\text{THD} = 10\log_{10}[(a_2^2+a_3^2+...)/a_1^2]. \qquad (7.2\text{-}1)$$

For lowpass filters the input signal frequency is chosen to be a sufficiently small fraction of the cutoff frequency for a reasonable number of harmonics to be included in the passband. Figure 7.2.3 shows the spectrum of the test board output for an input of 100mVrms/150kHz. The THD is 76.4dB. It should be noted that most of the noise spikes in this spectrum are not harmonics of the input signal, but electromagnetic interference picked up by the test board. For example, there is a signal of amplitude 48μV at frequency 810kHz which is almost certainly BBC Radio Scotland. Any spurious signal such as this present on the input of the board is amplified by 6dB due to the action of the single ended to differential converter.

Intermodulation distortion (IMD)

For bandpass filters it is not appropriate to measure the THD, since all of the harmonics of a signal within the passband will lie in the stopband and hence will be attenuated. A more meaningful measure of the linearity of a bandpass filter is intermodulation distortion. Two signals within the passband of the filter are summed and applied to the input. If the filter were perfectly linear then only these two components would be observed in the output. In practise some mixing (intermodulation) will occur causing the appearance of components with frequencies equal to the sums and differences of integer multiples of the two input frequencies. If the two input frequencies are f_1 and f_2, then the dominant IMD components lying within the passband will have frequencies equal to $(2f_1-f_2)$ and $(2f_2-f_1)$.

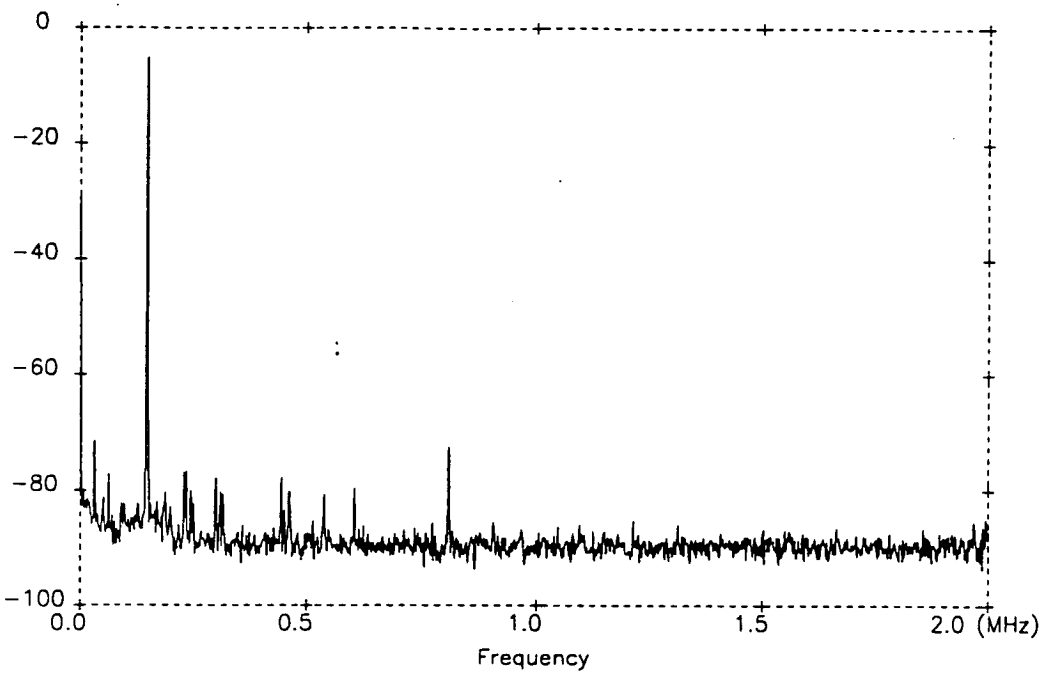


Figure 7.2-3 Output spectrum (in dB) of test board for a 100mVrms/150kHz sine input used to determine total harmonic distortion

Power Supply Rejection

A signal whose frequency lies within the CUT passband is superposed upon the positive power supply and the relative magnitude of the component of the differential output signal with this frequency is measured. The PSR of the test board alone is 47dB at 400kHz.

7.3 Lowpass filters

Measured results for two experimental lowpass filters are given in this section. The principal characteristics of these filters are summarised in table 7.3-1. The cutoff frequencies stated here are only nominal, since each filter can be tuned over a wide frequency range. The meanings of the transconductor acronyms along with appropriate circuit details can be found in this thesis at the page references shown in brackets.

Name	Cutoff Freq.	Order	Approximation	Transconductor	Page
LPF1	1MHz	5	elliptic	FCGMD (p 95)	162
LPF2	1MHz	5	elliptic	single stage GQ (p 81)	166

Table 7.3-1 Characteristics of experimental lowpass filters

For each filter the following information is given:

1 passive prototype ladder normalised to 1rad/sec cutoff frequency

2 fully differential transconductor ladder circuit, scaled to desired frequency

3 photomicrograph of fabricated circuit

4 graph of amplitude response

5 graph of measurement used to determine total harmonic distortion

6 table of designed and measured parameter values

Lowpass Filter 1 (LPF1)

The prototype for this fifth order elliptic lowpass filter (C0525 in [59]) is shown in figure 7.3-1.

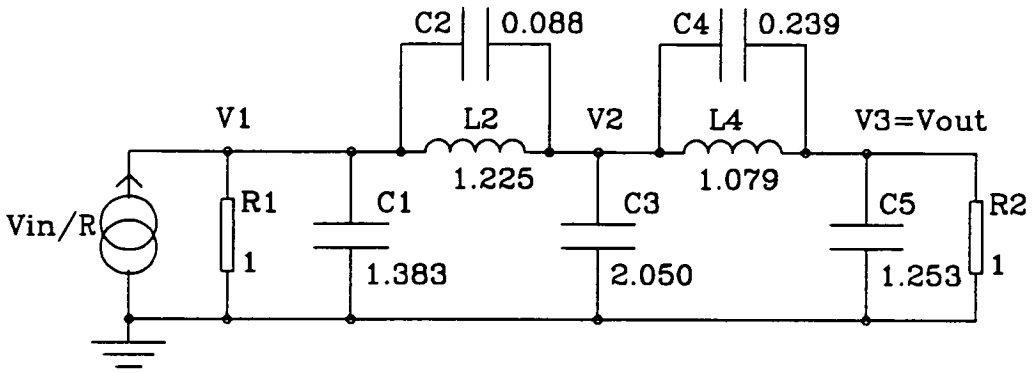


Figure 7.3-1 Passive prototype ladder for LPF1:

elliptic, 5th order, 0.28dB passband ripple, 60.5dB stopband attenuation

The active circuit was obtained, figure 7.3-2, by direct simulation of the nodal voltages and inductor currents of the prototype (section 3.2). The same topology could have been reached either by simulating the inductors with gyrators or by the Topological decomposition (section 6.2). The transconductor used is the folded cascode grounded quad transconductor described in chapter 5. Each of the transconductors with two pairs of inputs contain two grounded quads sharing a single cascode output stage and common mode feedback circuit. All of the load capacitors have their bottom plates grounded to disable their parasitics. (The different ways of configuring load capacitors were discussed in section 3.2.) Since conventional transconductors are used, the values of bottom plate parasitics of the floating capacitors have to be estimated and subtracted from the appropriate load capacitors.

The active circuit is scaled from a cutoff frequency of 1rad/sec to 1MHz by multiplying each transconductance by 10^{-4} (giving a nominal transconductance of 100μS) and each capacitor by $(2*\pi*10^{-4})/10^{6}$.

The measured performance of LPF1 is very satisfactory, table 7.3-2. The amplitude response, figure 7.3-4, is close to the designed shape with passband ripple and gain errors of only 0.12dB and 0.2dB respectively. The THD of 67.7dB compared favourably with many other transconductor filter results and indicates the success of the grounded quad cell for linear voltage to current conversion in low headroom applications.

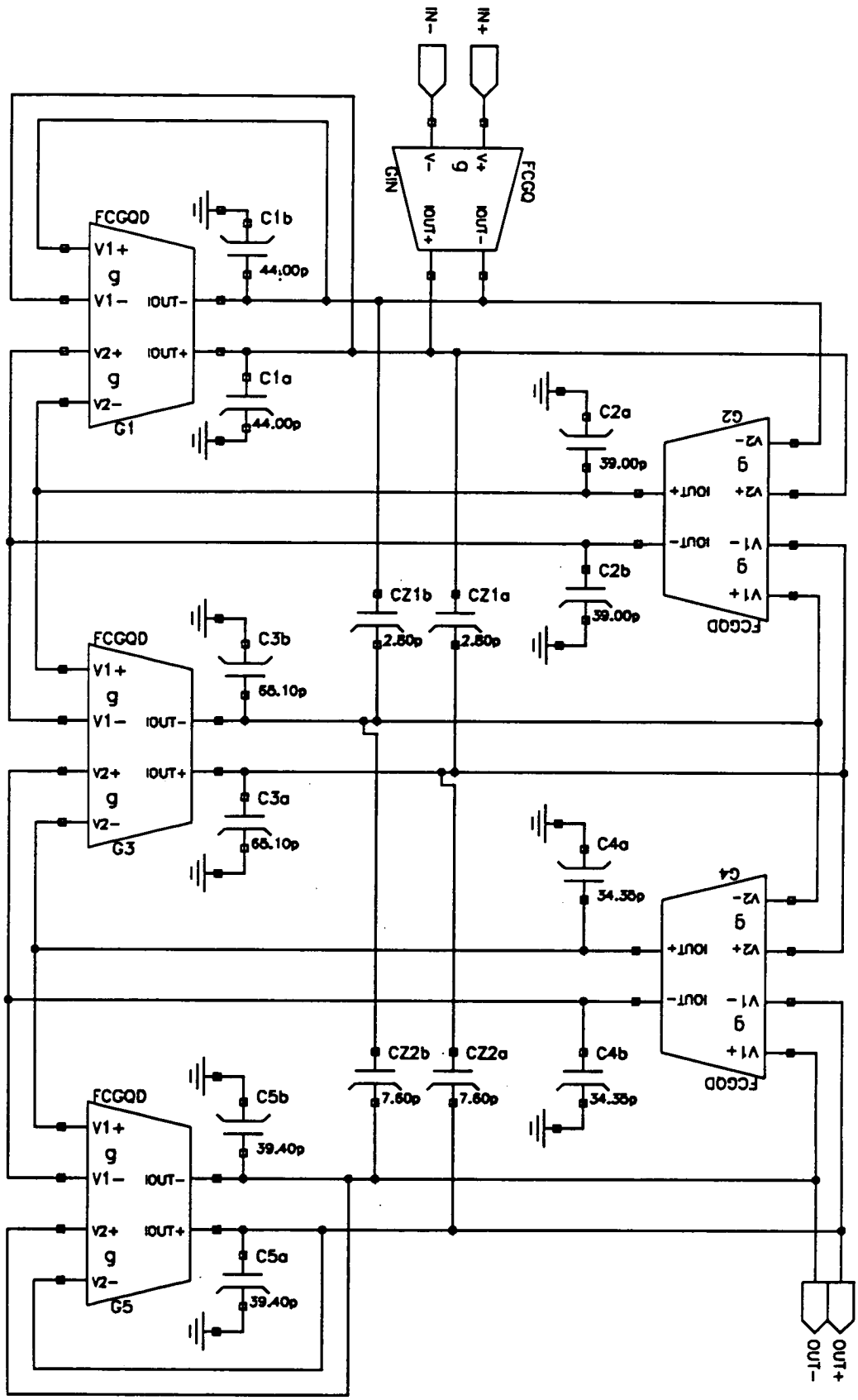


Figure 7.3-2 LPF1 fully differential schematic (bias lines omitted)

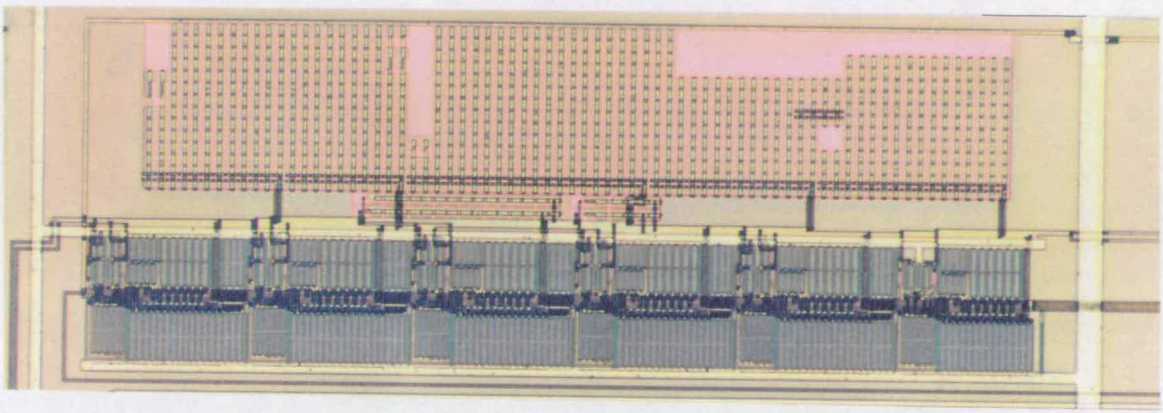


Figure 7.3-3 Photomicrograph of LPF1

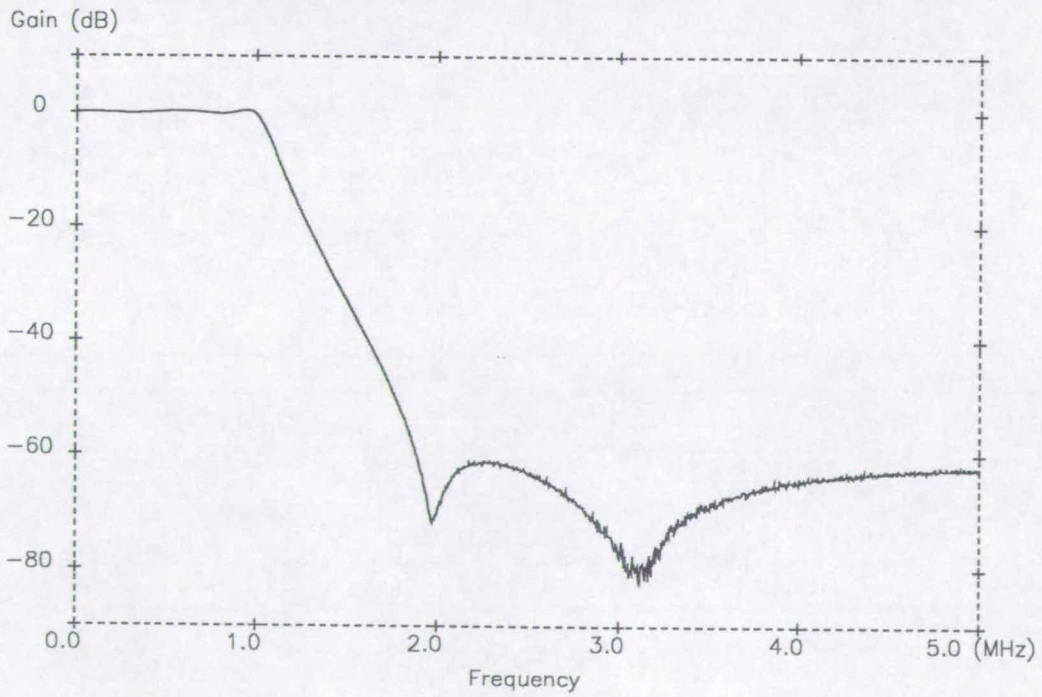


Figure 7.3-4 Measured amplitude response of LPF1

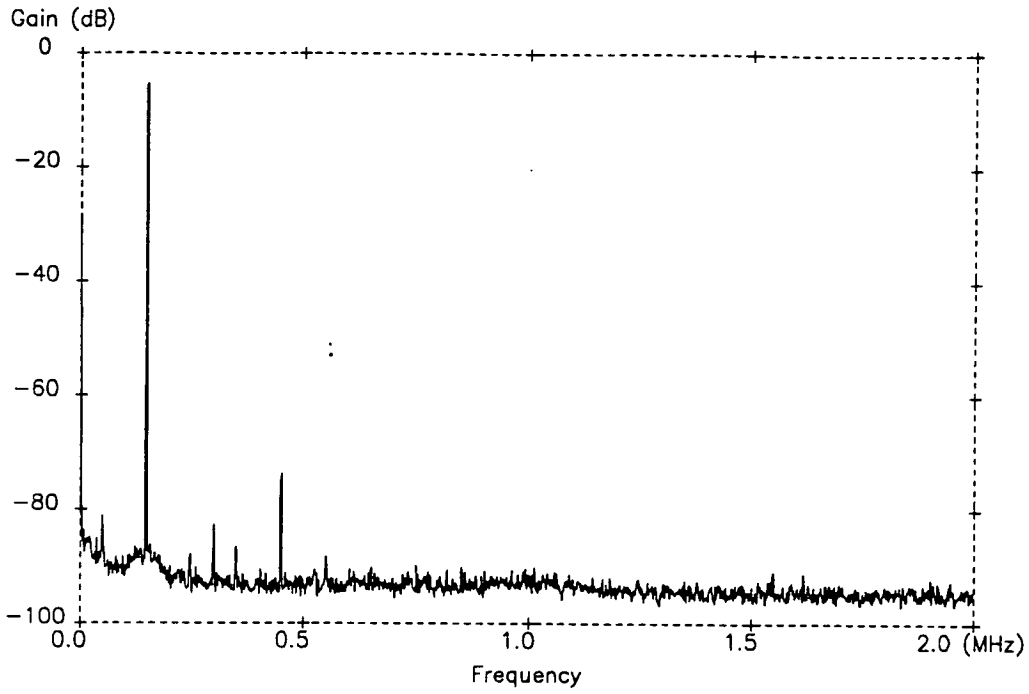


Figure 7.3-5 Spectrum of output of LPF1 used to determine harmonic distortion. The input signal is 250mVrms/150kHz. RBW = 100Hz.

Parameter	Designed	Measured
cutoff frequency	1MHz	
tuning range of cutoff freq.		250kHz-1.2MHz
passband gain	0dB	0.2dB
passband ripple	0.28dB	0.4dB
stopband attenuation	60dB	61.5dB
noise density in passband		$97nV/\sqrt{Hz}$
THD (200mVrms input)		-67.7dB
common mode rejection		71dB
cm to differential rejection		41dB
power supply rejection		43dB
current consumption	12.1mA	10mA

Table 7.3-2 Experimental results for LPF1

Lowpass Filter 2 (LPF2)

The design of LPF2 is identical to that of LPF1 except that single stage grounded quad transconductors are used (chapter 4) instead of the folded cascode version.

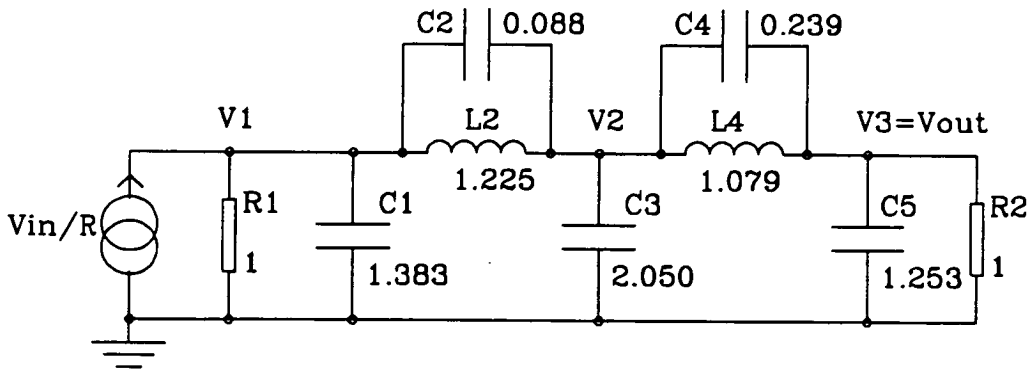


Figure 7.3-6 Passive prototype ladder for LPF2:

elliptic, 5th order, 0.28dB passband ripple, 60.5dB stopband attenuation

The transconductor ladder is shown in figure 7.3-7. The transconductors with two pairs of inputs contain two grounded quads sharing the same active load and common mode feedback circuit.

It is interesting to compare the measured parameters of LPF2 with those of LPF1. Not surprisingly the amplitude response of LPF2 is somewhat further from the designed shape. This is due to the low output impedance of the single stage transconductor causing phase lead in the integrators which form the ladder (appendix A). The fact that the distortion of the transfer function (in the frequency domain) is a *linear* phenomenon is emphasised by the fact that the THD of LPF2 is almost as good as that of LPF1. LPF2 is better than LPF1 in two respects. Firstly, the noise density in the passband is about 20% lower, which is to be expected since LPF2 has fewer transistors than LPF1 but has the same system node impedances. Secondly, the power and area consumption is lower.

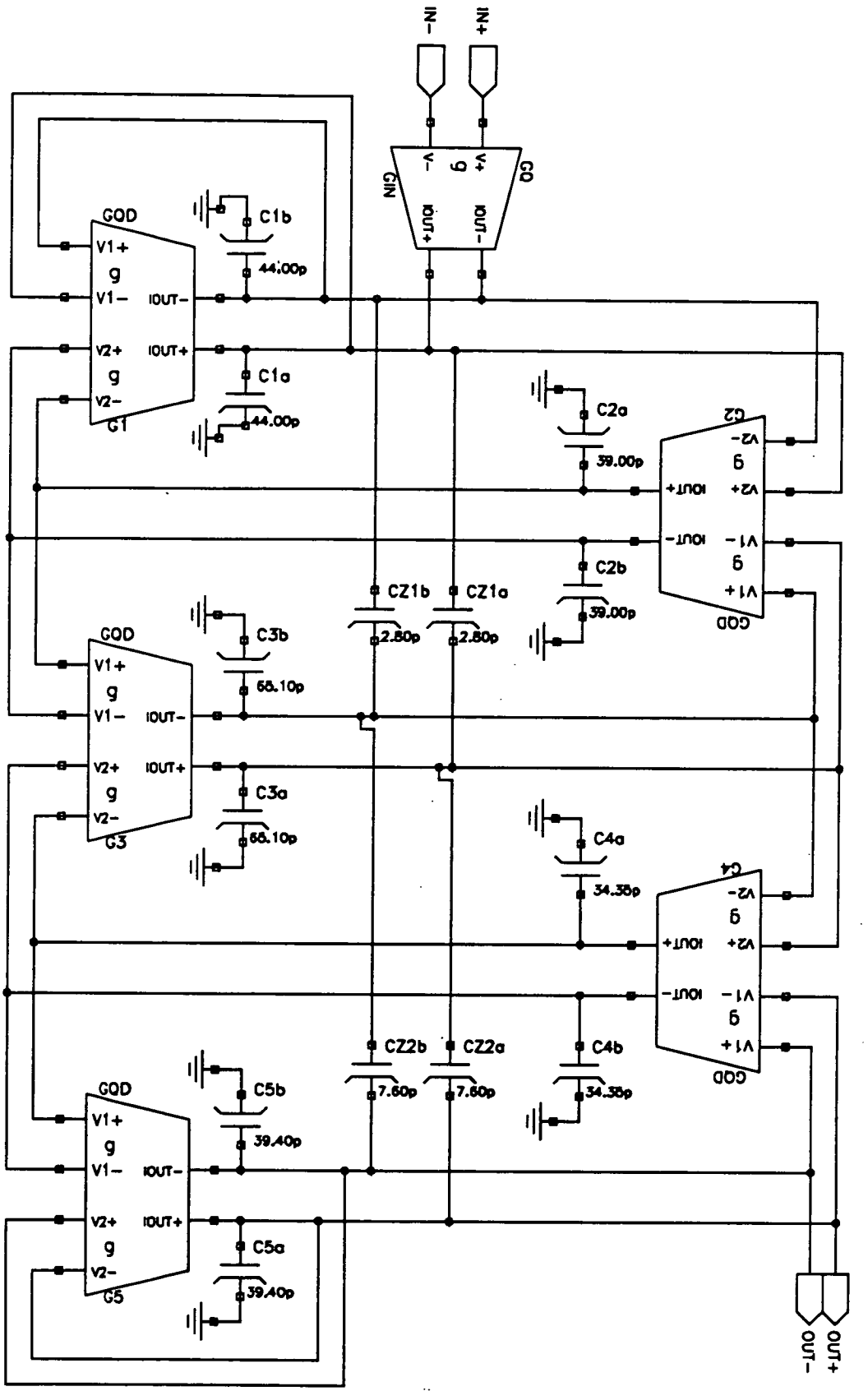


Figure 7.3-7 LPF2 fully differential schematic (bias lines omitted)

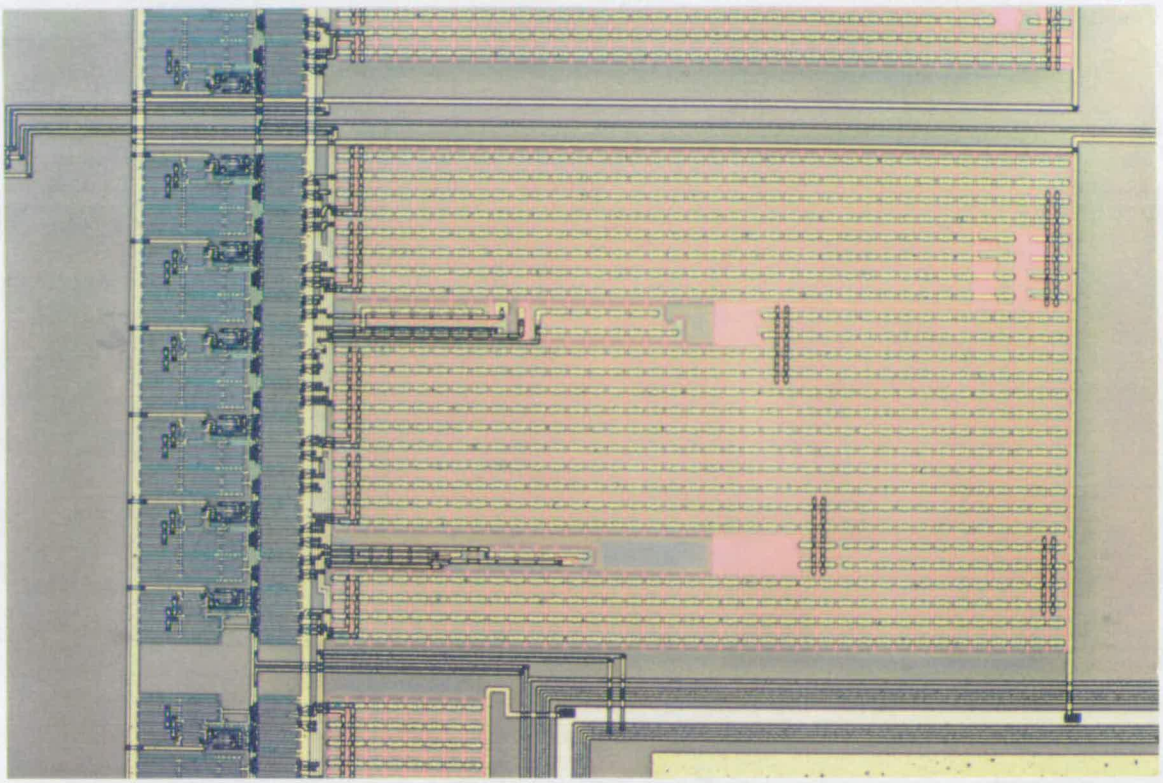


Figure 7.3-8 Photomicrograph of LPF2

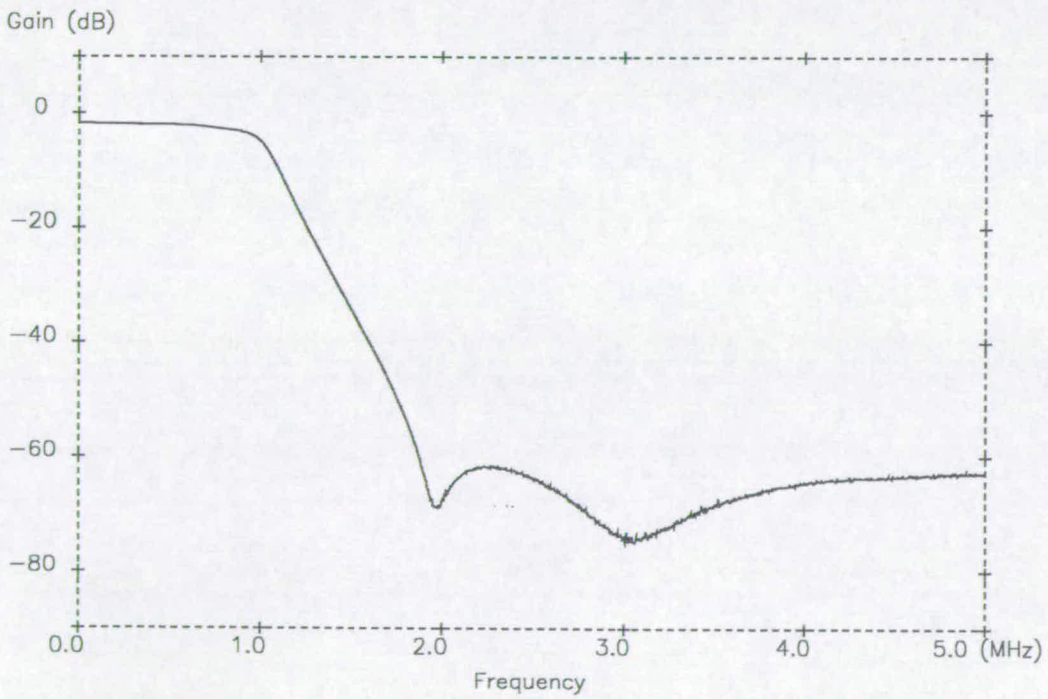


Figure 7.3-9 Measured amplitude response of LPF2

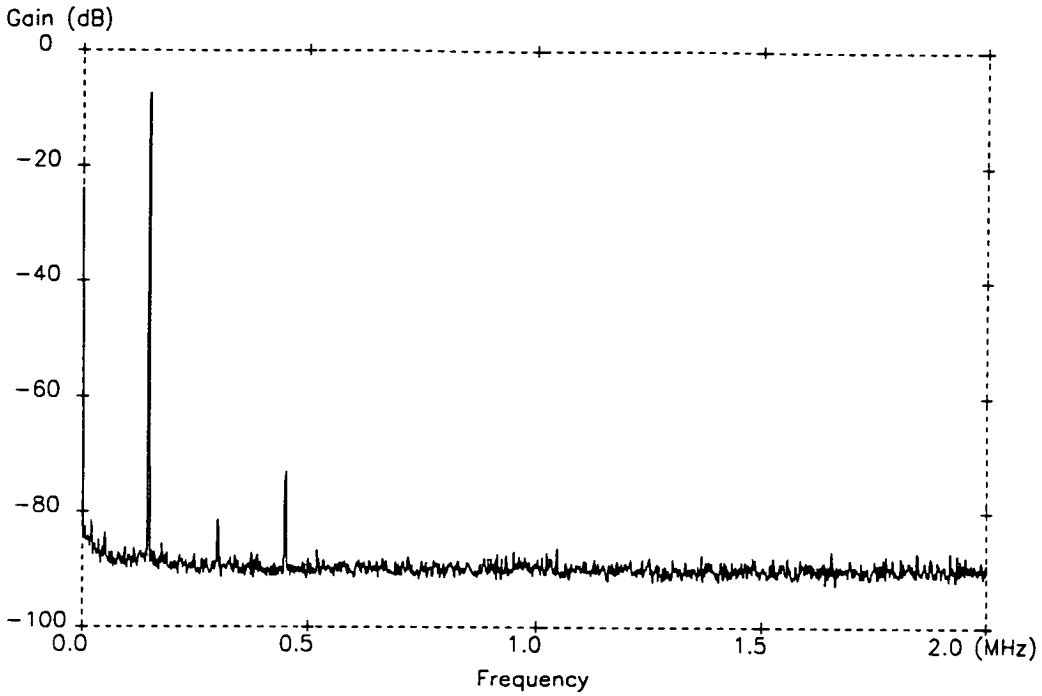


Figure 7.3-10 Spectrum of output of LPF2 used to determine harmonic distortion. The input signal has amplitude 250mV and frequency 150kHz. RBW = 100Hz.

Parameter	Designed	Measured
cutoff frequency	1MHz	
tuning range of cutoff freq.		250kHz-1.2MHz
passband gain	0dB	-2dB
passband ripple	0.28dB	3dB
stopband attenuation	60dB	59.9dB
noise density in passband		$80nV/\sqrt{Hz}$
THD (200mVrms input)		-65.1dB
common mode rejection		71dB
cm to differential rejection		45dB
power supply rejection		46dB
current consumption	7.6mA	7.8mA

Table 7.3-3 Experimental results for LPF2

7.4 Bandpass filters

Measured results for six experimental bandpass filters are given in this section. The principal characteristics of these filters are summarised in table 7.4-1. The centre frequencies stated here are only nominal, since each filter can be tuned over a wide frequency range. The meanings of the transconductor acronyms along with appropriate circuit details can be found in this thesis at the page references shown in brackets.

Name	Centre Freq.	BW	Approx.	Transconductor	Page
BPF1	400kHz	10%	Chebyshev	FCGM (p 91)	172
BPF2	400kHz	10%	Chebyshev	FCGM (p 91) + buffered o/p	176
BPF3	400kHz	10%	Chebyshev	FCGM + low Z i/p (p 104)	180
BPF4	455kHz	1.6%	Chebyshev	FC GQ + low Z i/p (p 104)	184
BPF5	1MHz	10%	Chebyshev	FCGM (p 91)	188
BPF6	400kHz	10%	elliptic	FCGM (p 91)	192

Table 7.4-1 Characteristics of experimental bandpass filters

The first three filters have the same amplitude specification but use different methods to realise the termination branches. The first is the conventional ratioed transconductor method, as described in chapter 3. The second and third use only a single value of transconductor since they have unidirectional capacitive branches, introduced by output buffers and low impedance inputs respectively.

The fourth filter has a very narrow bandwidth (1.6%). In this case ratioed transconductors cannot be used since the narrow passband would force an impracticably large ratio to be used. Instead a single value of transconductor with low impedance inputs is used so that the unidirectional damping branches can be realised with capacitors.

The fifth filter is identical to BPF1, except that it is scaled to a higher nominal centre frequency.

The last filter has an elliptic response and was designed using one of the matrix methods introduced in the previous chapter (the Right Inverse decomposition).

The five Chebyshev filters are "asymmetric" in the sense that the two

stopbands of the transfer function do not have the same magnitude of gradient when viewed on a logarithmic frequency axis. The asymmetric response was chosen because it can be realised using a prototype ladder which has only *capacitors* coupling the LC resonators. This restricts the possible use of a second value of transconductance to the termination branches. A classical "symmetric" prototype would have a coupling inductor in place of capacitor C_4. After the filters described here were submitted for fabrication it was realised that even a symmetric all-pole filter can be realised easily, using the Left Direct or Right Inverse matrix methods as described in section 6.3.

For each filter the following information is given:

1 passive prototype ladder normalised to 1rad/sec centre frequency,

2 fully differential transconductor ladder circuit, scaled to desired frequency,

3 photomicrograph of fabricated circuit,

4 graph of amplitude response,

5 graph of measurement used to determine intermodulation distortion,

6 table of designed and measured parameter values.

Bandpass Filter 1 (BPF1)

This filter demonstrates the first of three ways of developing an active ladder from the prototype shown in figure 7.4-1.

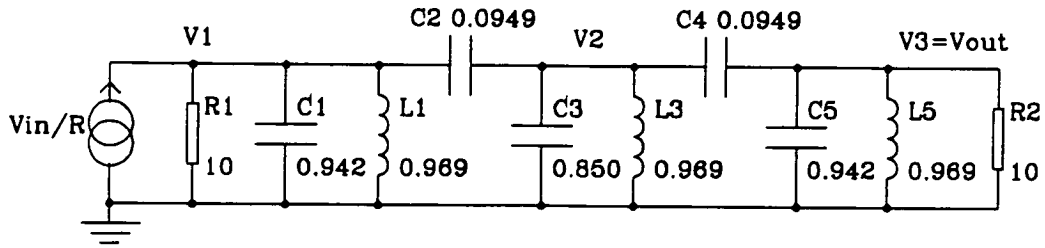


Figure 7.4-1 Prototype ladder: Chebyshev, 10% bandwidth, 0.1dB passband ripple

The active ladder, using the folded cascode grounded quad transconductor is shown in figure 7.4-2. Each inductor is simulated using a gyrator (section 3.2) with capacitive load. Each termination resistor is simulated by a transconductor with its outputs connected to its inputs of opposite polarity. To scale the nodal voltages correctly, the transconductors forming the gyrators have a value (g = 100μS) ten times that of the termination transconductors (g/10 = 10μS). Normally in this direct simulation approach, the input branch would also be realised with a transconductive input to GV1 of value g/10 (or g/5 if 0dB gain at centre frequency is desired). However this transconductance is avoided by using a part of the capacitive load of GX1. The output voltage of GX1 is then the superposition of a voltage proportional to the current in the prototype inductor L1 plus a fraction of the input voltage. This simple trick is only possible because the filter has zero transmission at d.c. and because the output voltage of GX1 is referred to only by another transconductor's input (and not a bidirectional capacitive branch). It makes the assumption that the input voltage is delivered by a source whose impedance is much less than that of the input capacitors in the frequency range of interest.

The amplitude response of BPF1 is shown in figure 7.4-4. This measurement was made with the frequency control loop in operation, with clock frequency fc=950kHz. The noise spike in the upper stopband at 1.9MHz is breakthrough from the output of the phase lock loop's phase detector which drives the off-chip loop filter.

The measurement used to determine intermodulation distortion is shown in figure 7.4-5. It is clear from this graph that one of the signal generators used is considerably more noisy than the other.

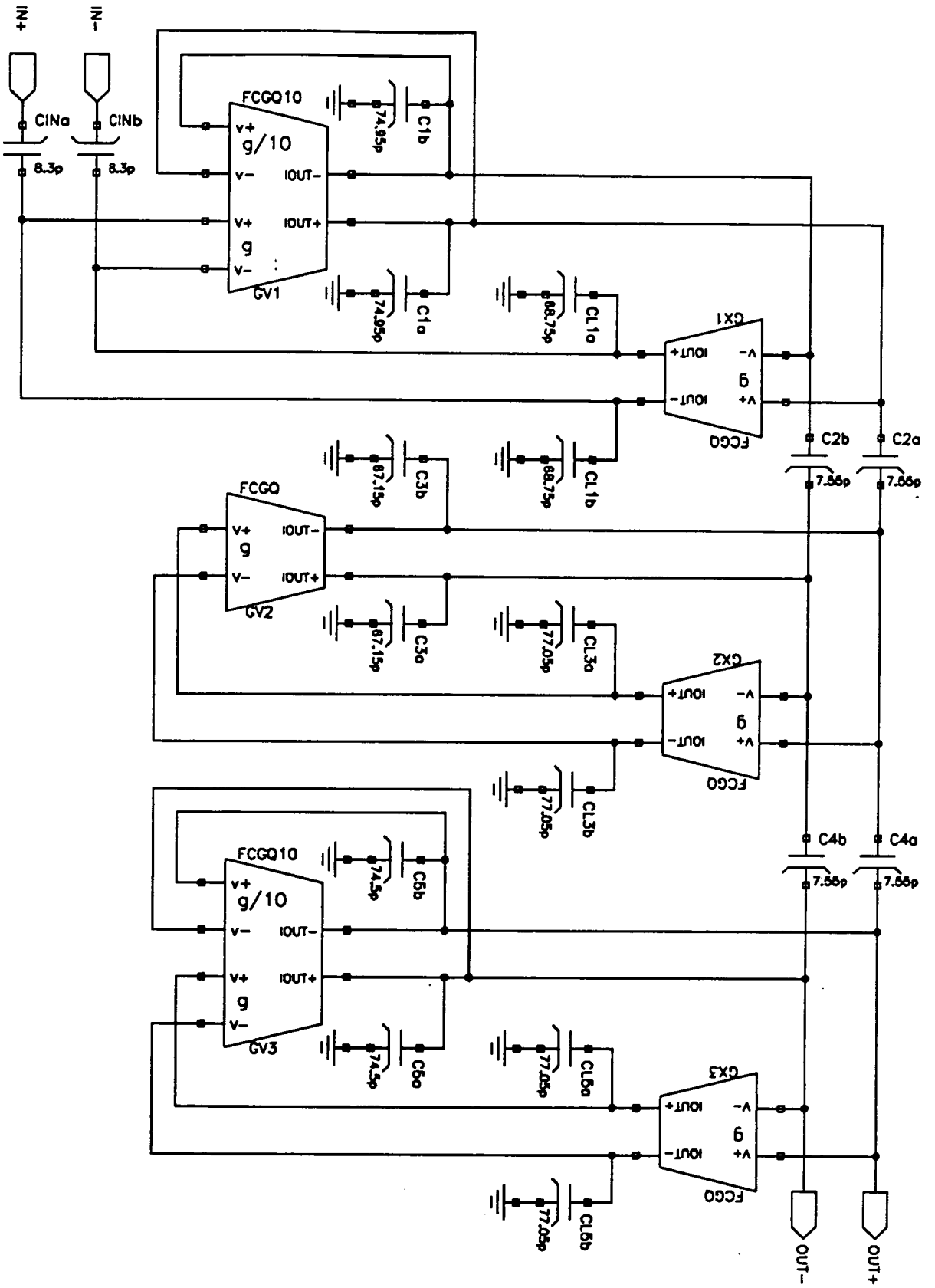


Figure 7.4-2 BPF1 fully differential schematic (bias lines omitted); g = 100μS

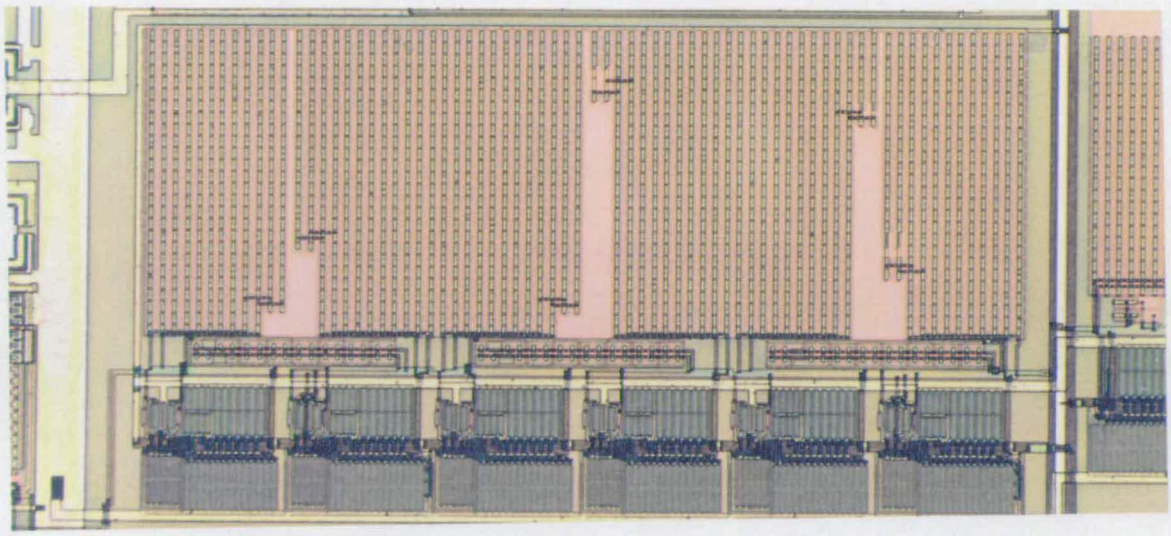


Figure 7.4-3 Photomicrograph of BPF1

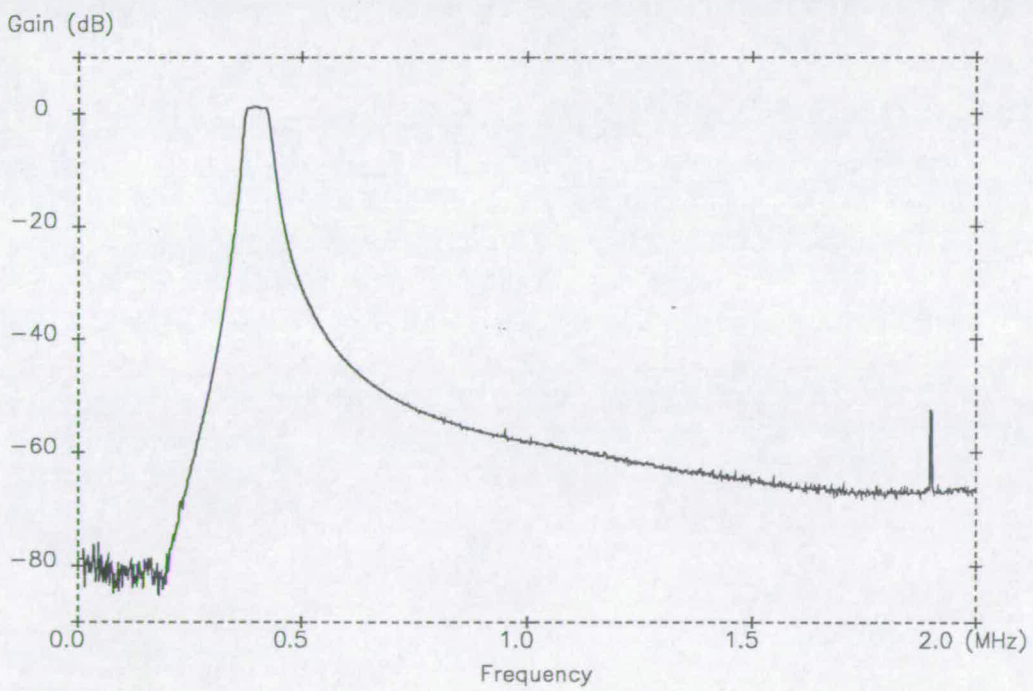


Figure 7.4-4 Measured amplitude response of BPF1

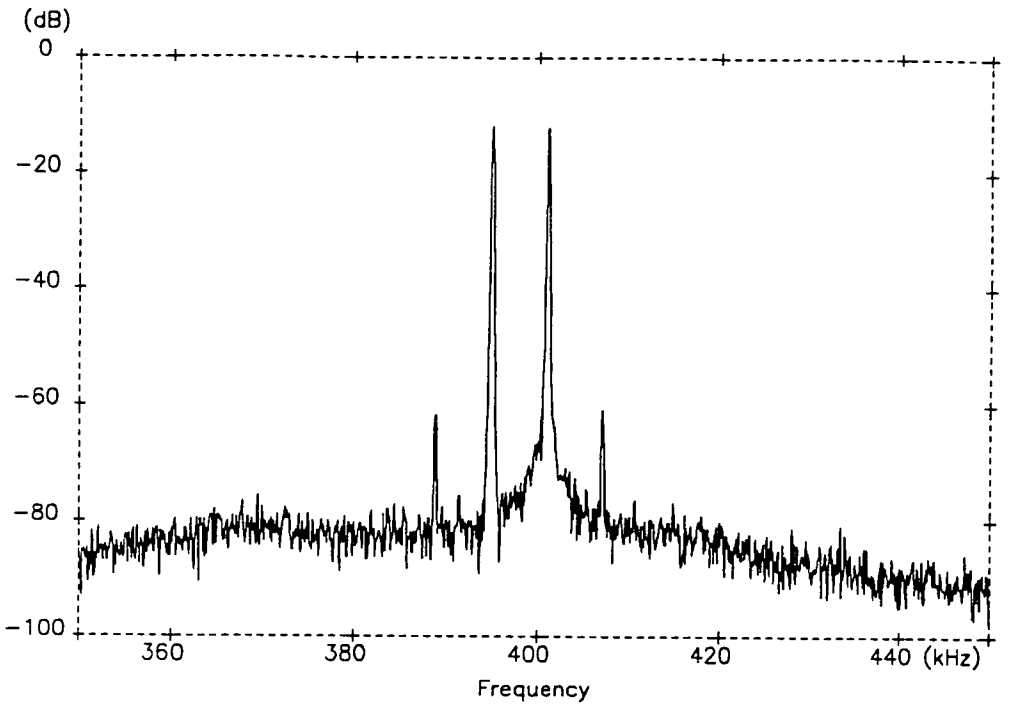


Figure 7.4-5 Spectrum of output of BPF1 used to determine intermodulation distortion. The two input terms are 100mVrms/395kHz and 100mVrms/401kHz

Parameter	Designed	Measured
centre frequency	400kHz	
tuning range of centre freq.		80kHz-530kHz
bandwidth	10%	10%
passband gain	0dB	1.1dB
passband ripple	0.1dB	0.31dB
noise density in passband		840nV/$\sqrt{\text{Hz}}$
ref. signal breakthrough		390μV
intermodulation distortion		-48.5dB
common mode rejection		76dB
cm to differential rejection		44dB
power supply rejection		45dB
current consumption	9.2mA	11.3mA

Table 7.4-2 Experimental results for BPF1

Bandpass Filter 2 (BPF2)

We refer to the previous filter as an "F-type" ladder since the termination branches are realised directly by resistive (transconductive in this case) elements; by analogy with the terminations and terminology used in a well known class of switched capacitor biquads [6]. In contrast, this and the following filter can be called "E-type" since they use non-integrating capacitive paths to realise the termination branches. Of course these branches have to be unidirectional so one plate of each damping capacitor has to be connected to a low impedance node. In BPF3 this is effected by using the transconductor with low impedance inputs which was introduced in chapter 5. In BPF2 however the low impedance nodes are created by buffering the output voltages of the appropriate transconductors. In the transconductor ladder, figure 7.4-7, each buffer is depicted as a triangle containing the symbol 1. The buffer is very simple, consisting of two transistors: a source follower biased by a single transistor current sink.

This method of implementing capacitive damping branches was suggested several years ago, but was rejected on the grounds that there would inevitably be a few degrees of phase shift through the voltage buffer which would cause distortion of the filter transfer function [24,27]. That criticism may be true, however the effect cannot be severe in the present design, as shown by the results in table 7.4-3.

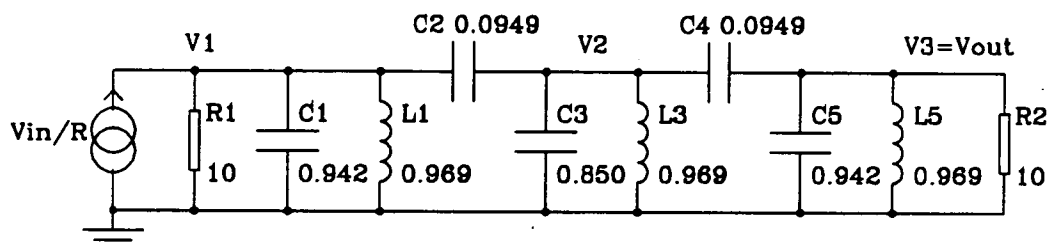


Figure 7.4-6 Passive prototype ladder for BPF2:
asymmetric Chebyshev, 10% bandwidth, 0.1dB passband ripple

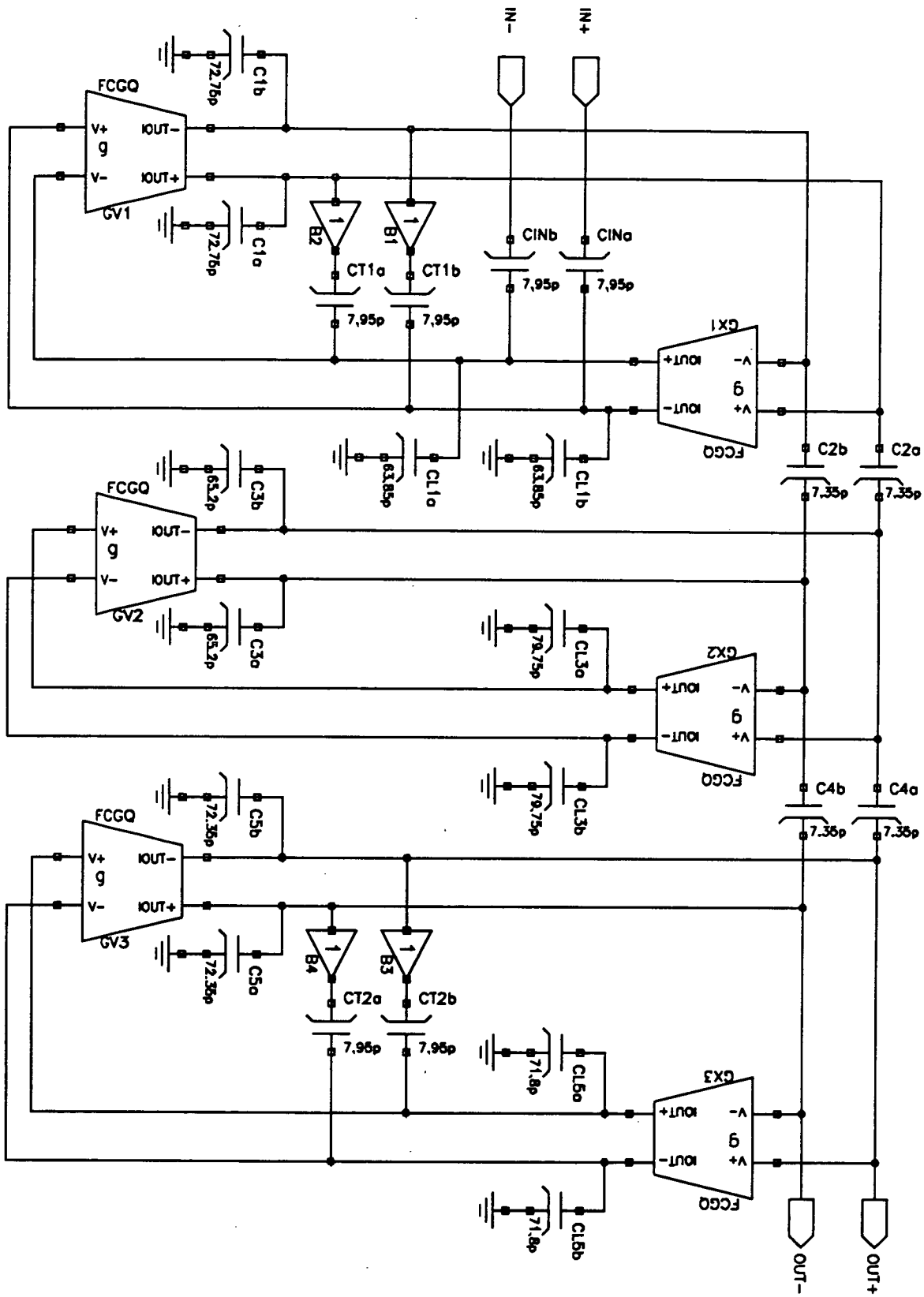


Figure 7.4-7 BPF2 fully differential schematic (bias lines omitted)

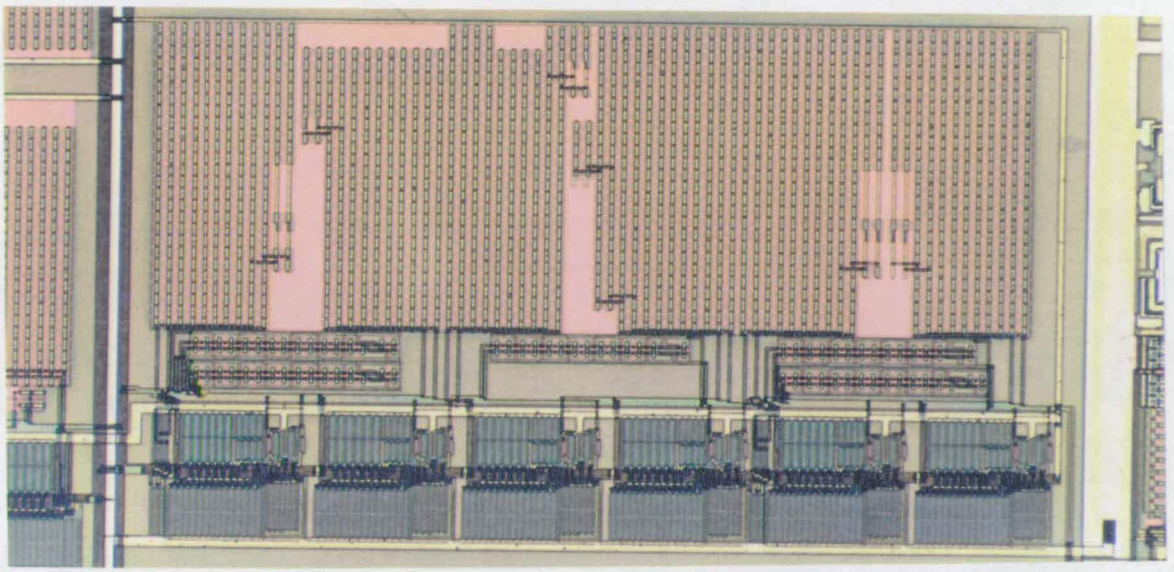


Figure 7.4-8 Photomicrograph of BPF2

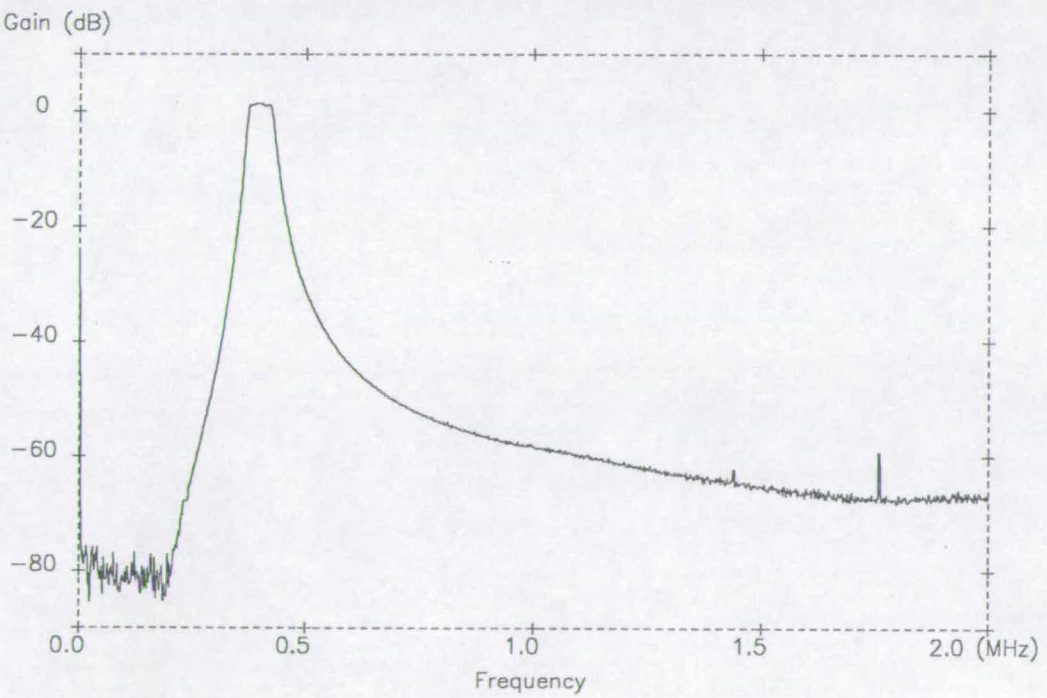


Figure 7.4-9 Measured amplitude response of BPF2

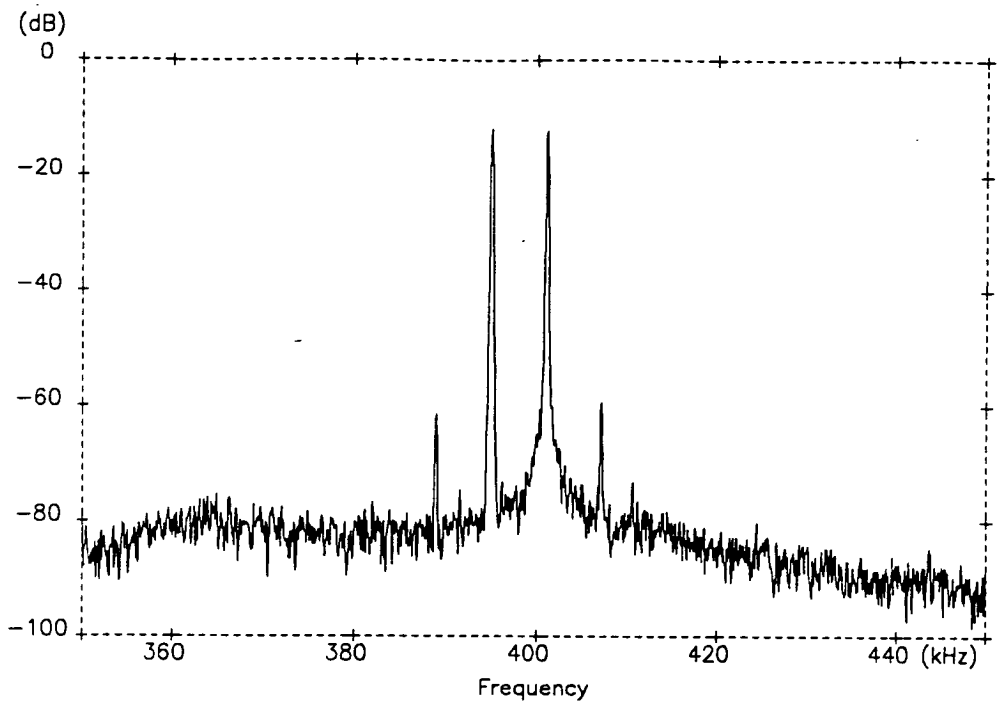


Figure 7.4-10 Spectrum of output of BPF2 used to determine intermodulation distortion. The two input terms are 100mVrms/395kHz and 100mVrms/401kHz

Parameter	Designed	Measured
centre frequency	400kHz	
tuning range of centre freq.		110kHz-525kHz
bandwidth	10%	11%
passband gain	0dB	1.5dB
passband ripple	0.1dB	0.57dB
noise density in passband		$1.05\mu V/\sqrt{Hz}$
ref. signal breakthrough		342μV
intermodulation distortion		47.7dB
common mode rejection		74dB
cm to differential rejection		44dB
power supply rejection		54dB
current consumption	9.5mA	11.2mA

Table 7.4-3 Experimental results for BPF2

Bandpass Filter 3 (BPF3)

This filter is another E-type ladder, using capacitive termination branches and only a single value of transconductance. The termination branches are made unidirectional by use of transconductors with low impedance inputs (chapter 5).

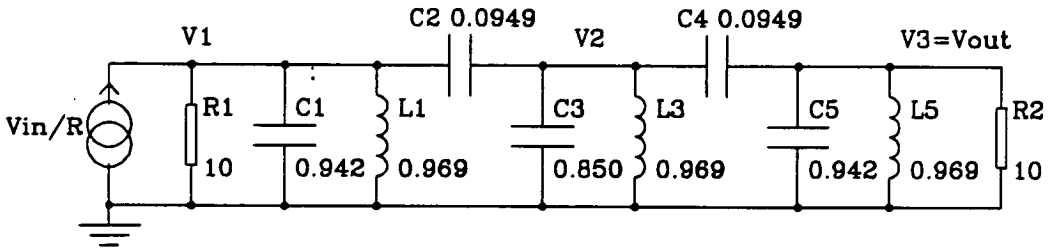


Figure 7.4-11 Passive prototype ladder for BPF3:
asymmetric Chebyshev, 10% bandwidth, 0.1dB passband ripple.

The measured performance of this filter, table 7.4-4, is generally similar to the data obtained from BPF1 and BPF2 which are alternative realisations of the same transfer function.

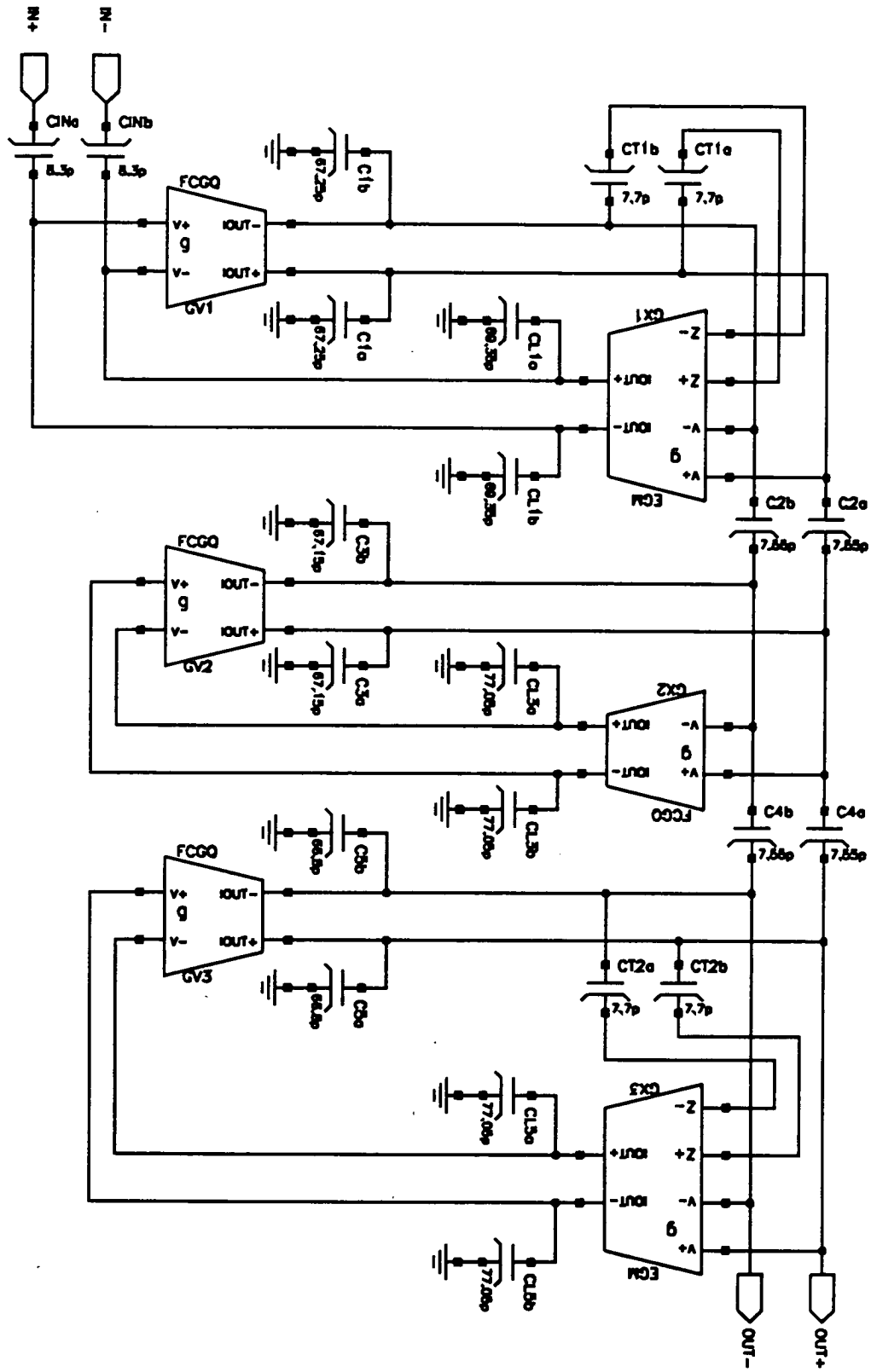


Figure 7.4-12 BPF3 fully differential schematic (bias lines omitted)

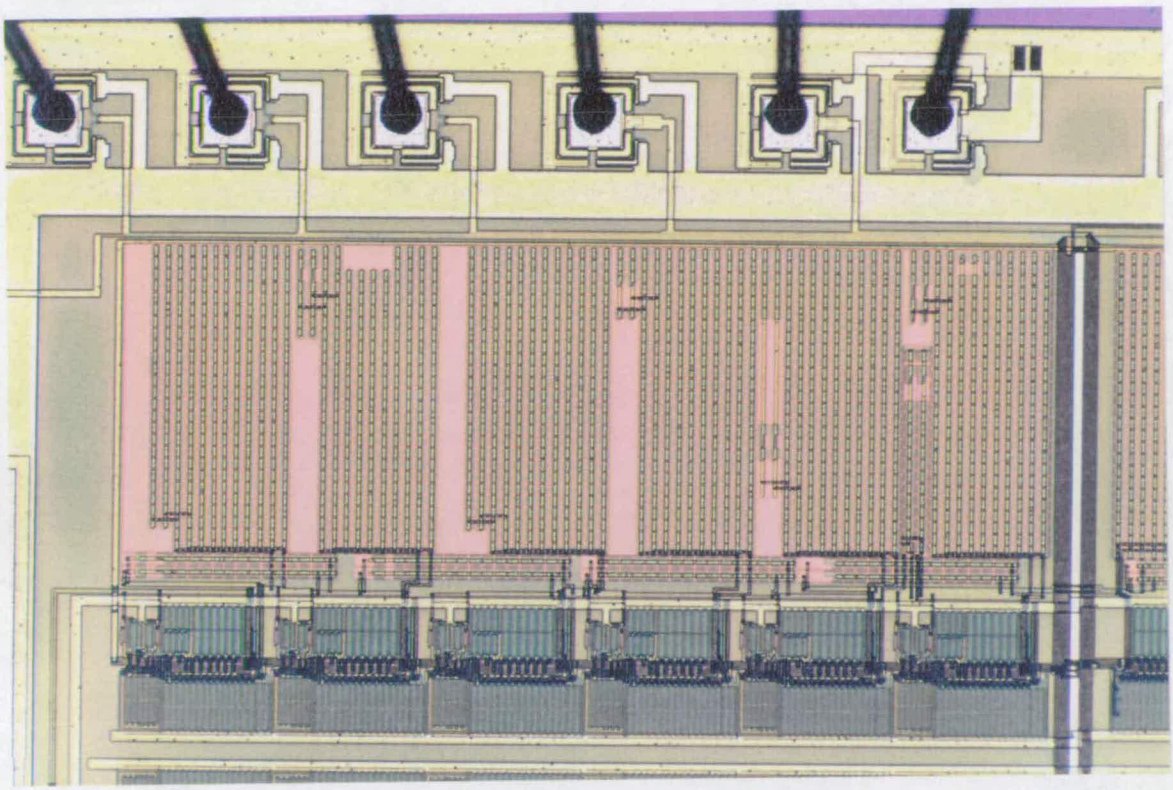


Figure 7.4-13 Photomicrograph of BPF3

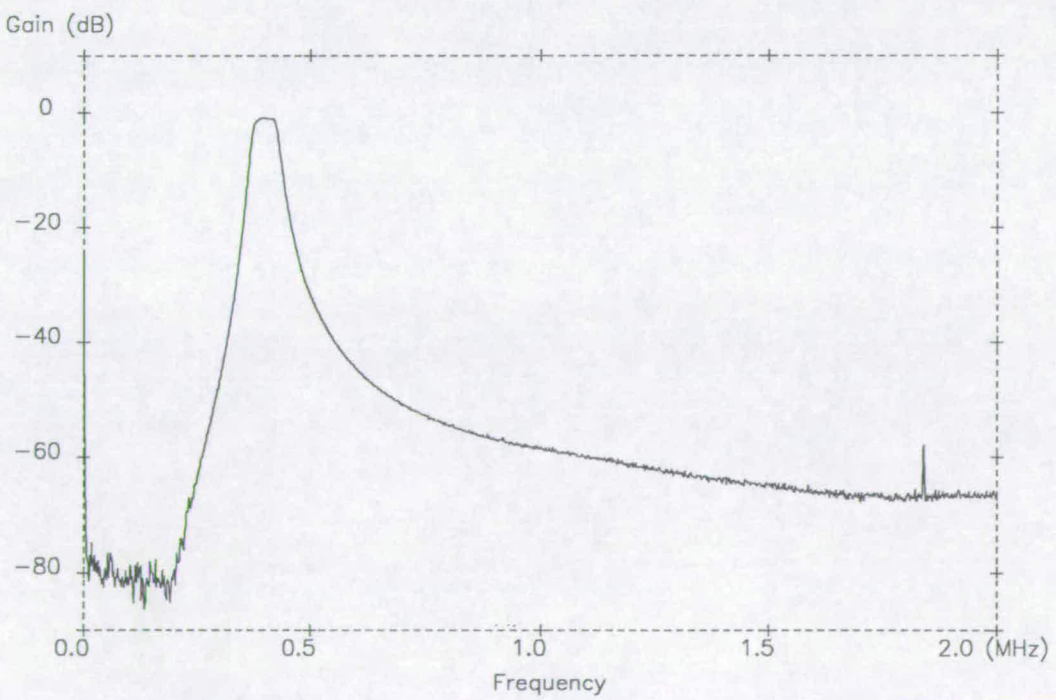


Figure 7.4-14 Measured amplitude response of BPF3

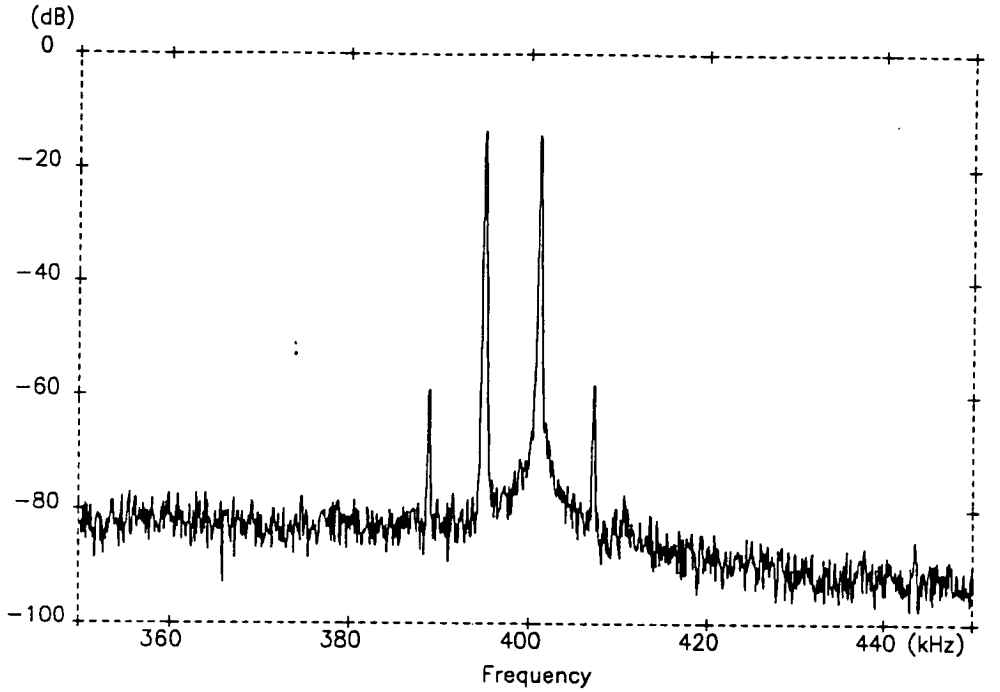


Figure 7.4-15 Spectrum of output of BPF3 used to determine intermodulation distortion. The two input terms are 100mVrms/395kHz and 100mVrms/401kHz

Parameter	Designed	Measured
centre frequency	400kHz	
tuning range of centre freq.		100kHz-550kHz
bandwidth	10%	10%
passband gain	0dB	-0.9dB
passband ripple	0.1dB	1dB
noise density in passband		$920nV/\sqrt{Hz}$
ref. signal breakthrough		200μV
intermodulation distortion		-48.7dB
common mode rejection		72dB
cm to differential rejection		43dB
power supply rejection		46dB
current consumption	9.7mA	11.6mA

Table 7.4-4 Experimental results for BPF3

Bandpass Filter 4 (BPF4)

BPF4 has a much narrower bandwidth than the other bandpass filters reported in this chapter. The specification of 7kHz bandwidth and 455kHz centre frequency (which is very challenging for a filter on silicon) is similar to that of a typical intermediate filter in an AM radio. The topology of the prototype, figure 7.4-16, is identical to that of the wider band filter used in the design of the previous three filters, however the component values are different. Most noticeably the coupling capacitors C_2 and C_4 have a lower value, as would be expected for a more selective filter.

For such a narrow band filter it is not practical to use an F-type ladder with conventional transconductors because nodal voltage scaling would force a very large transconductance ratio (in the region of 65:1). So this is an example of the utility of the low impedance inputs in a transconductor. Figure 6.4-17 shows the E-type ladder using only a single value of transconductance.

Figure 6.4-19 shows the measured amplitude response of BPF4. It should be noted that whereas all the other results presented in this chapter are typical for the CUT concerned, the results for this filter are those of the best sample. In general the measured transfer function of BPF4 shows a significant degree of distortion. The fact that transfer function varies from sample to sample indicates that the source of error is random rather than systematic. Therefore the problem is more likely to be one of mismatch between the grounded quads in the transconductors than, say, excess phase. A narrower band filter is more susceptible to mismatch because it has poles placed very close together in the frequency domain as a result of which a pole error of certain absolute value will take effect as a large relative error. Problems due to transconductor phase errors are also more pronounced in narrower band filters, however as stated above they do not appear to be dominant in this case.

A tighter tolerance on this filter might be achieved by paying more attention to layout. For example the grounded quads (which set the transconductance values) could be brought out of the transconductors and placed closer together, possibly using spatial averaging (common centroid) techniques.

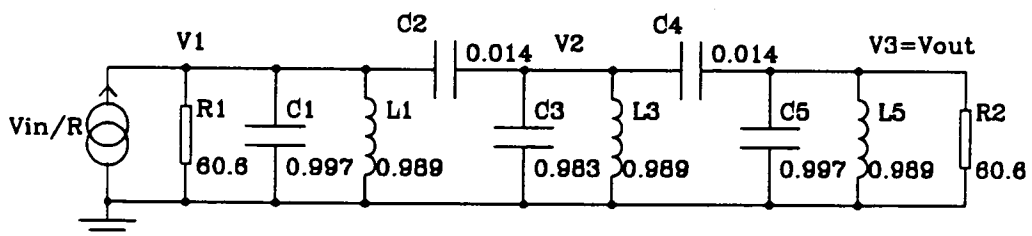


Figure 7.4-16 Prototype for BPF4: asymmetric Cheb., 1.65% BW, 0.1dB ripple.

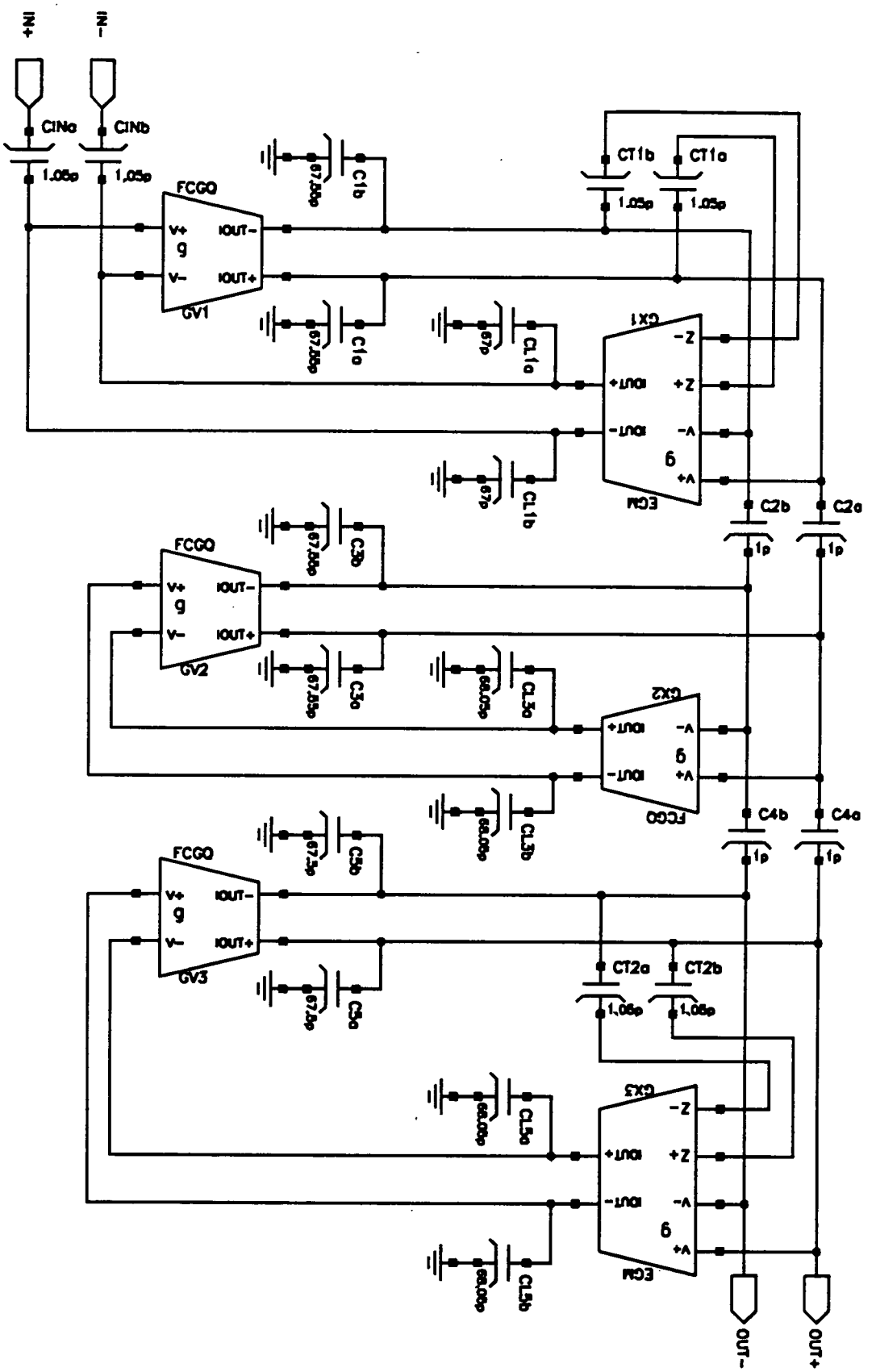


Figure 7.4-17 BPF4 fully differential schematic (bias lines omitted)

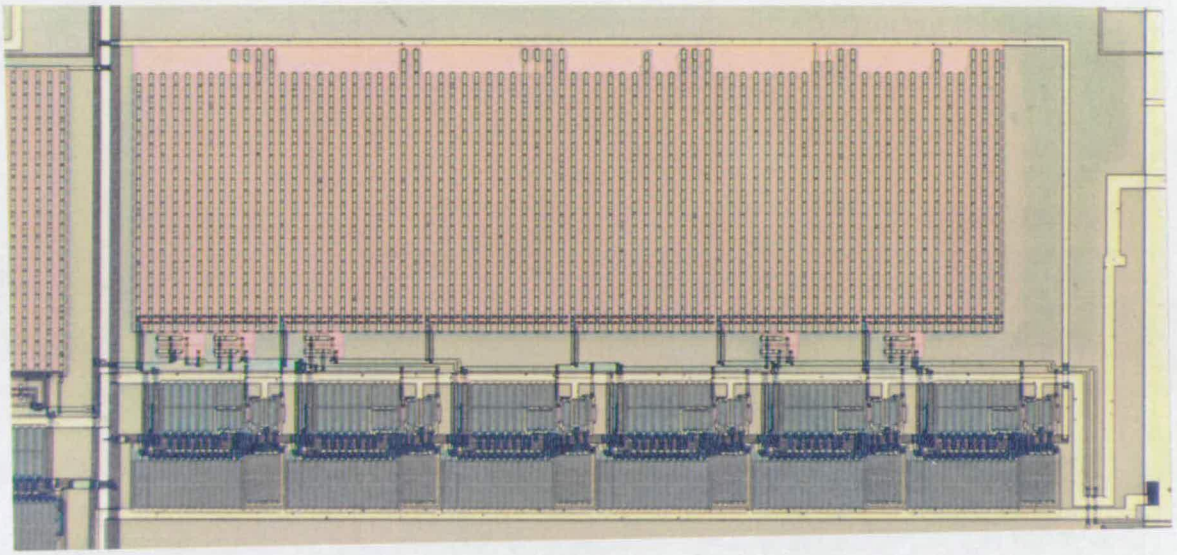


Figure 7.4-18 Photomicrograph of BPF4

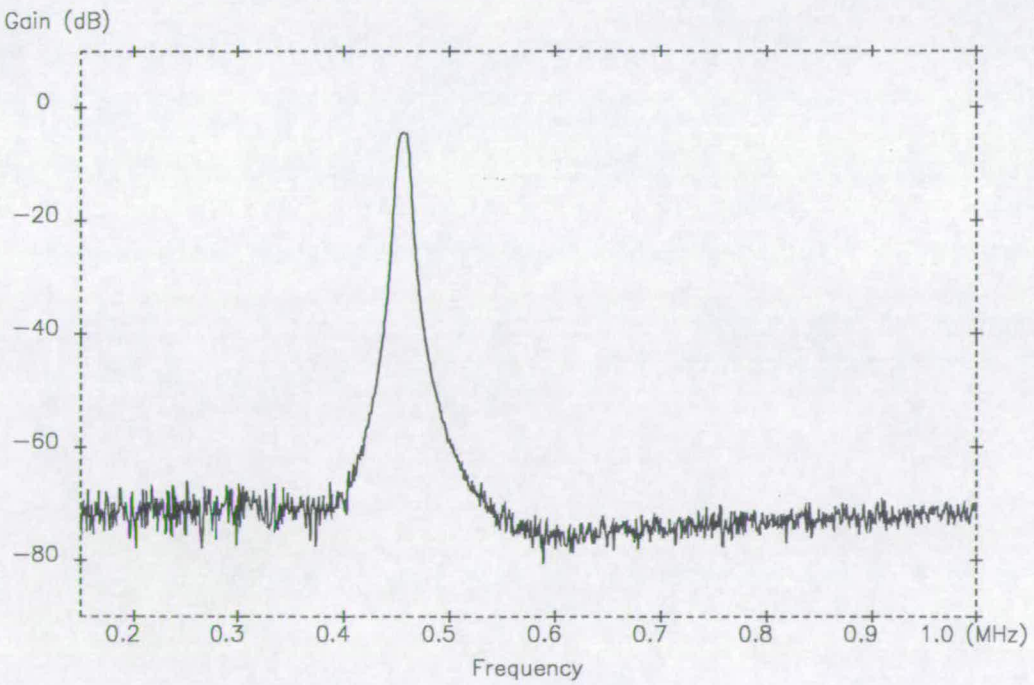


Figure 7.4-19 Measured amplitude response of BPF4

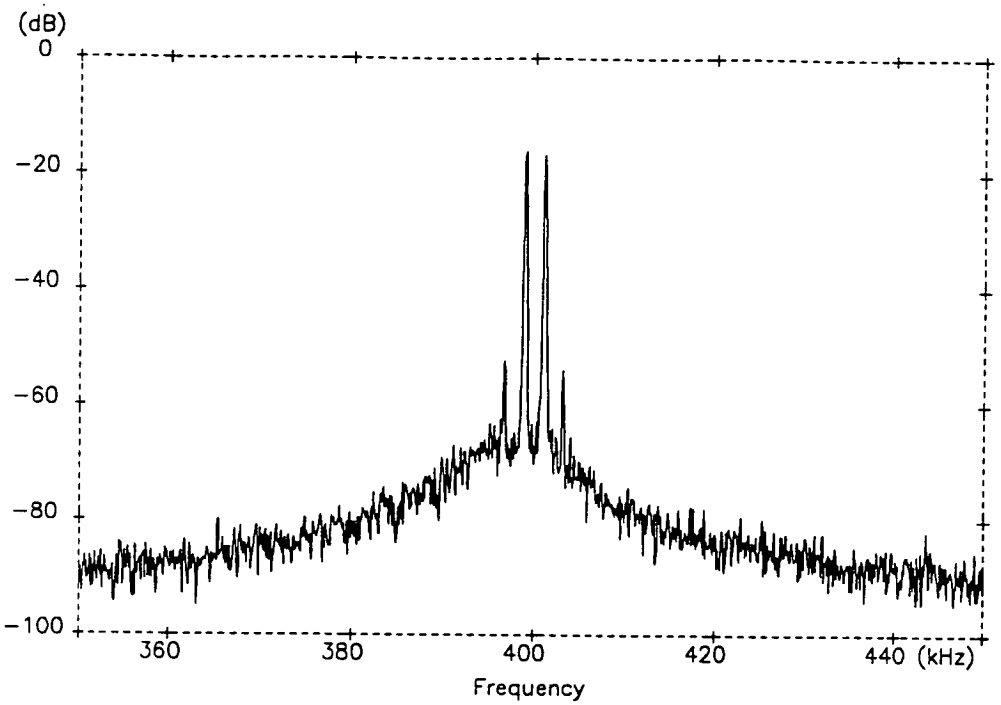


Figure 7.4-20 Spectrum of output of BPF4 used to determine intermodulation distortion. The two input terms are 100mV/399kHz and 100mV/401kHz

Parameter	Designed	Measured
centre frequency	400kHz	
tuning range of centre freq.		200kHz-640kHz
bandwidth	7kHz	6kHz
passband gain	0dB	-4.1dB
passband ripple	0.1dB	0.3dB
noise density in passband		$4.5\mu V/\sqrt{Hz}$
ref. signal breakthrough		200μV
intermodulation distortion		-36.7dB
common mode rejection		75dB
cm to differential rejection		44dB
power supply rejection		42dB
current consumption	9.7mA	11.2mA

Table 7.4-5 Experimental results for BPF4

Bandpass Filter 5 (BPF5)

This filter is the same as BPF1, but scaled to a centre frequency of 1MHz. The transconductor ladder is shown in figure 7.4-22. The scaling from BPF1 is performed by dividing each capacitor value by 2.5.

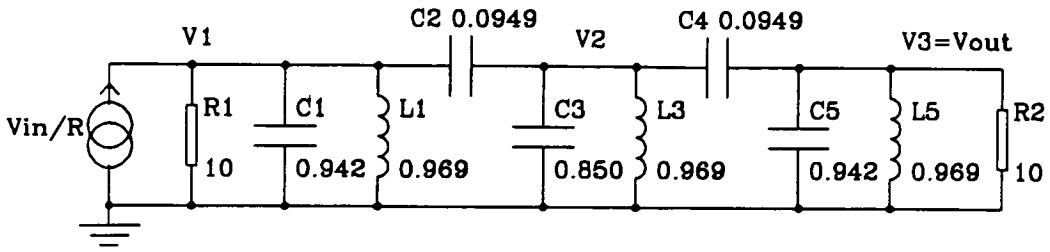


Figure 7.4-21 Passive prototype ladder for BPF5:
asymmetric Chebyshev, 10% bandwidth, 0.1dB passband ripple

The measured amplitude response, figure 7.4-24, is as good as those of the 400kHz filters. This suggests that the same transconductor might be used in bandpass filters with even high centre frequencies (several MHz) without excess phase problems becoming serious.

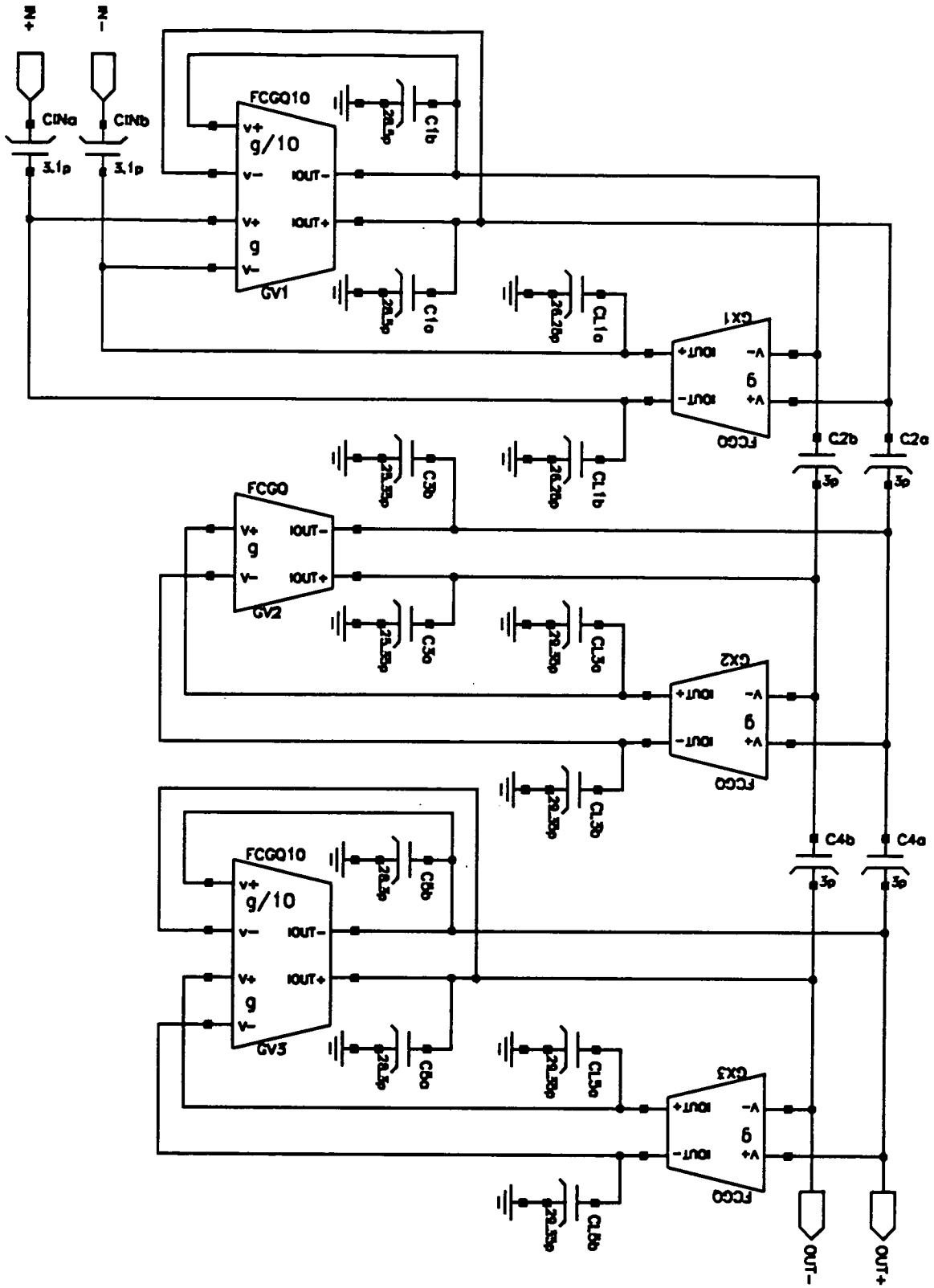


Figure 7.4-22 BPF5 fully differential schematic (bias lines omitted)

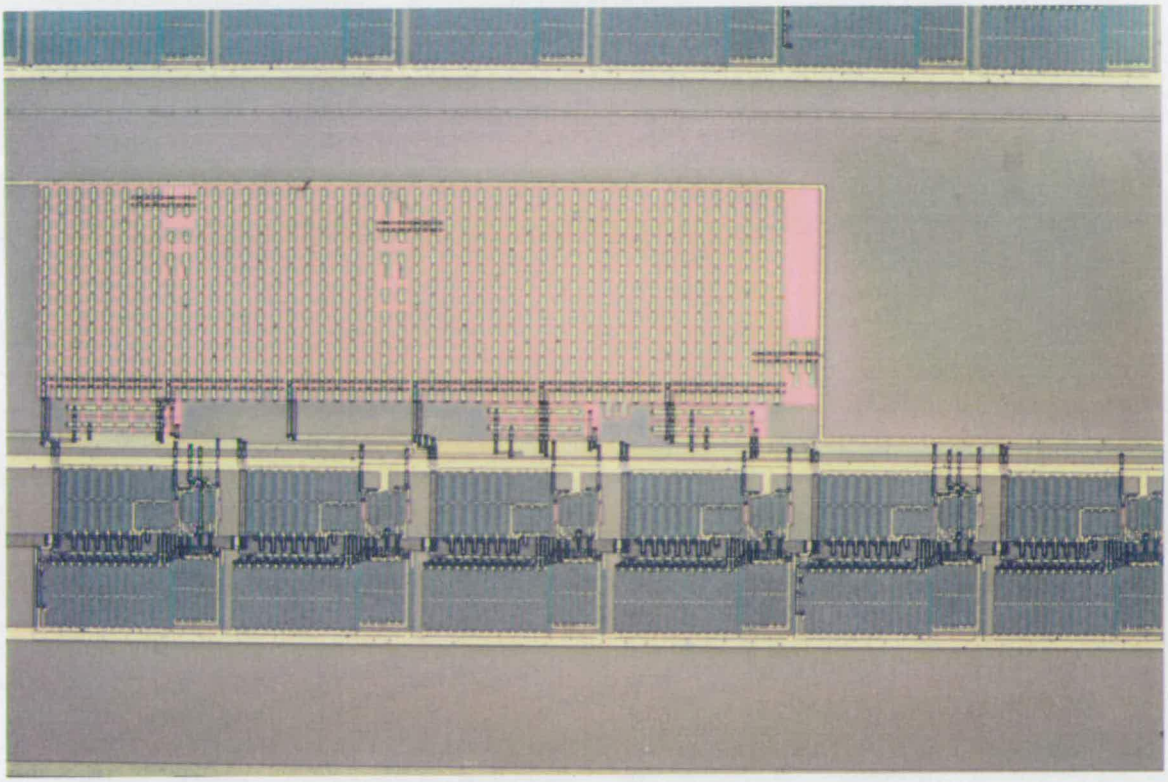


Figure 7.4-23 Photomicrograph of BPF5

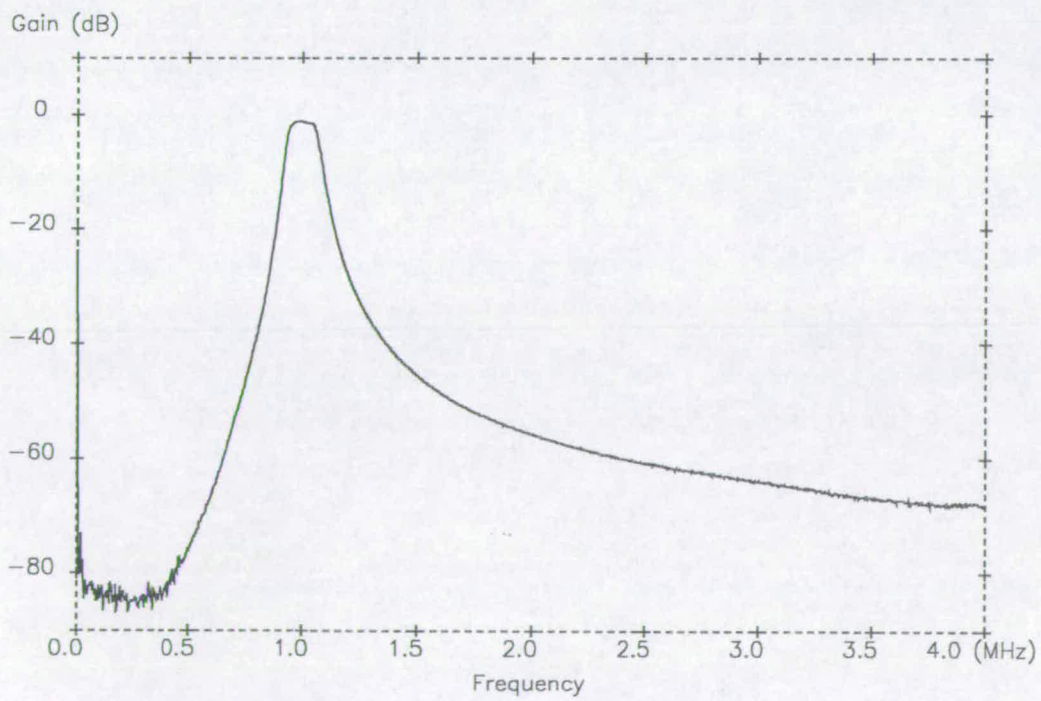


Figure 7.4-24 Measured amplitude response of BPF5

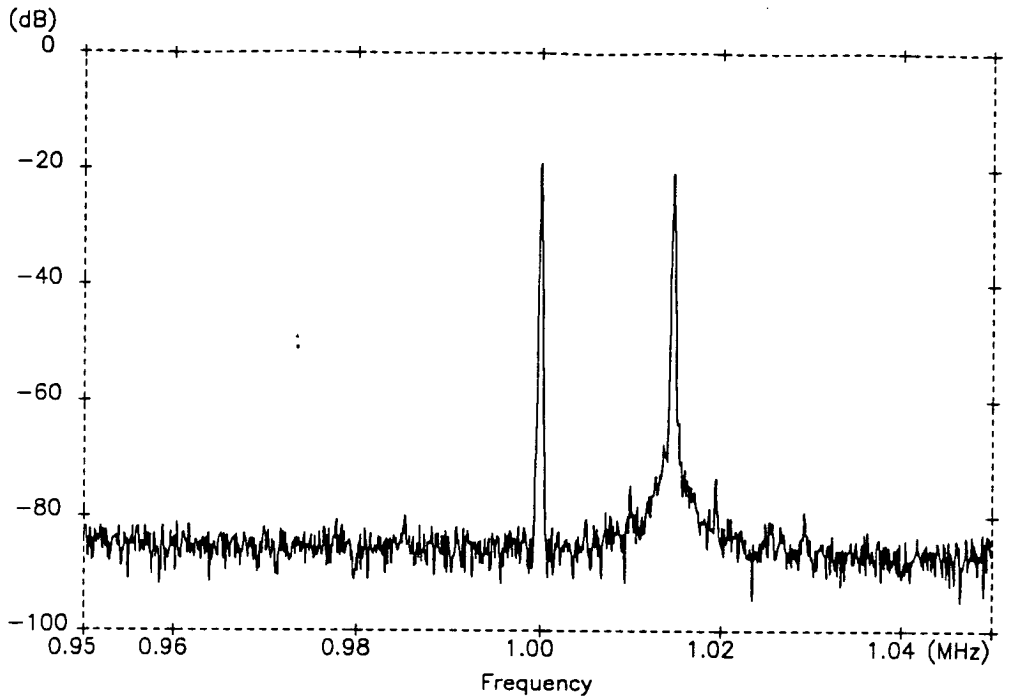


Figure 7.4-25 Spectrum of output of BPF5 used to determine intermodulation distortion. The two input terms are 60mV/1.0MHz and 50mV/1.015MHz

Parameter	Designed	Measured
centre frequency	1MHz	
tuning range of centre freq.		700kHz-1.2MHz
bandwidth	10%	10%
passband gain	0dB	-1.2dB
passband ripple	0.1dB	0.7dB
noise density in passband		620nV/$\sqrt{\text{Hz}}$
intermodulation distortion		-56.9dB
common mode rejection		81.3dB
cm to differential rejection		43dB
power supply rejection		42dB
current consumption	9.2mA	8.8mA

Table 7.4-6 Experimental results for BPF5

Bandpass Filter 6 (BPF6)

This is an example of a filter the design of which would not be feasible without the algebraic method described in chapter 6. The sixth order elliptic prototype, figure 7.4-26, contains two closed inductor loops and any attempt to simulate it using gyrators or inductor current simulation would lead to an active circuit which is either unstable or full of unfeasible transconductor ratios.

Instead, the Right Inverse decomposition is used as described in section 6.3, giving an active ladder which requires only two values of conventional transconductor: 100μS in the resonators and 10μS in the input and damping branches. This is shown in figure 7.4-27; for the sixth order case the RI decomposition does not lead to an excessive degree of interconnect. As usual, the values of the bottom plate parasitics of all the floating capacitors are subtracted from the appropriate grounded capacitors.

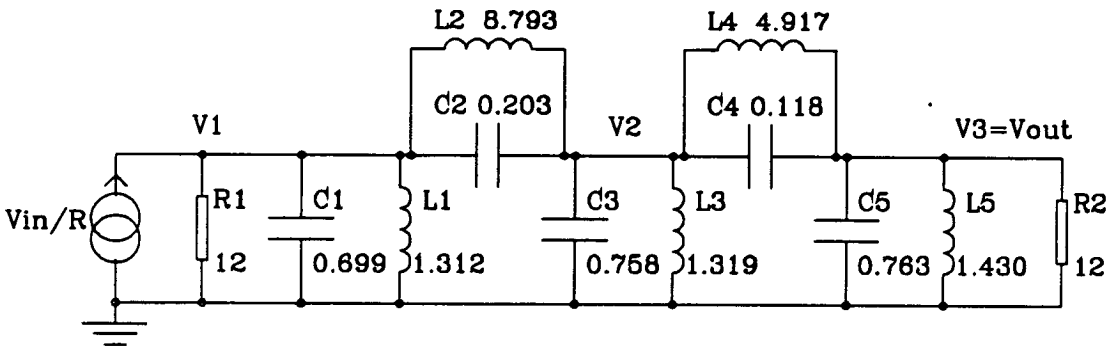


Figure 7.4-26 Passive prototype ladder for BPF6:

elliptic, 10% bandwidth, 0.1dB passband ripple, 50dB stopband attenuation

The measured amplitude response of BPF6 is shown in figure 7.4-29. This shows close agreement with the designed transfer function, with the exception of the lower frequency edge which has a slight attenuation, the cause of which is not yet known. The linearity, figure 7.4-30, is similar to that of the Chebyshev filters, as might be expected.

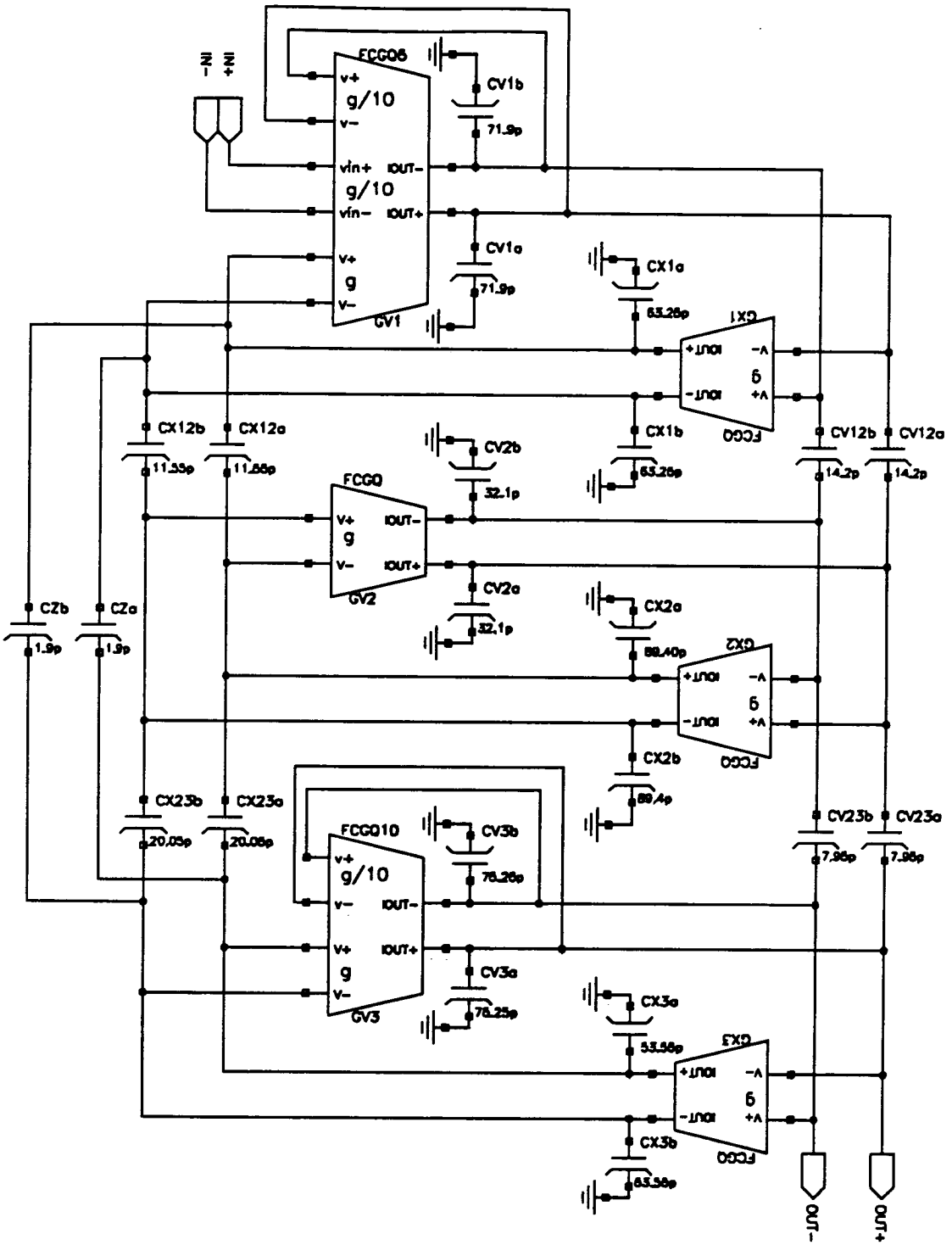


Figure 7.4-27 BPF6 fully differential schematic (bias lines omitted)

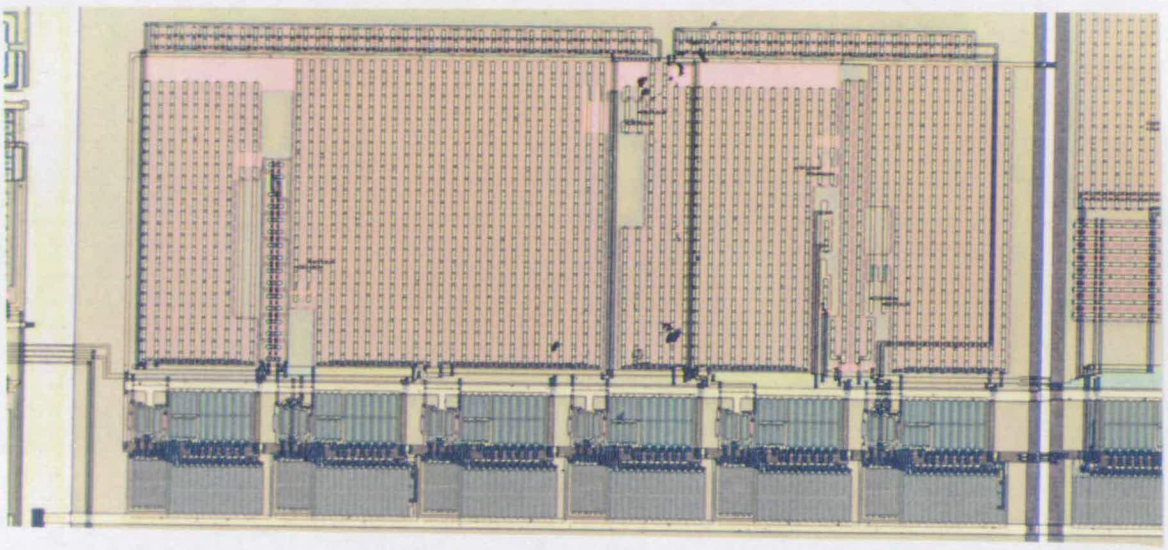


Figure 7.4-28 Photomicrograph of BPF6

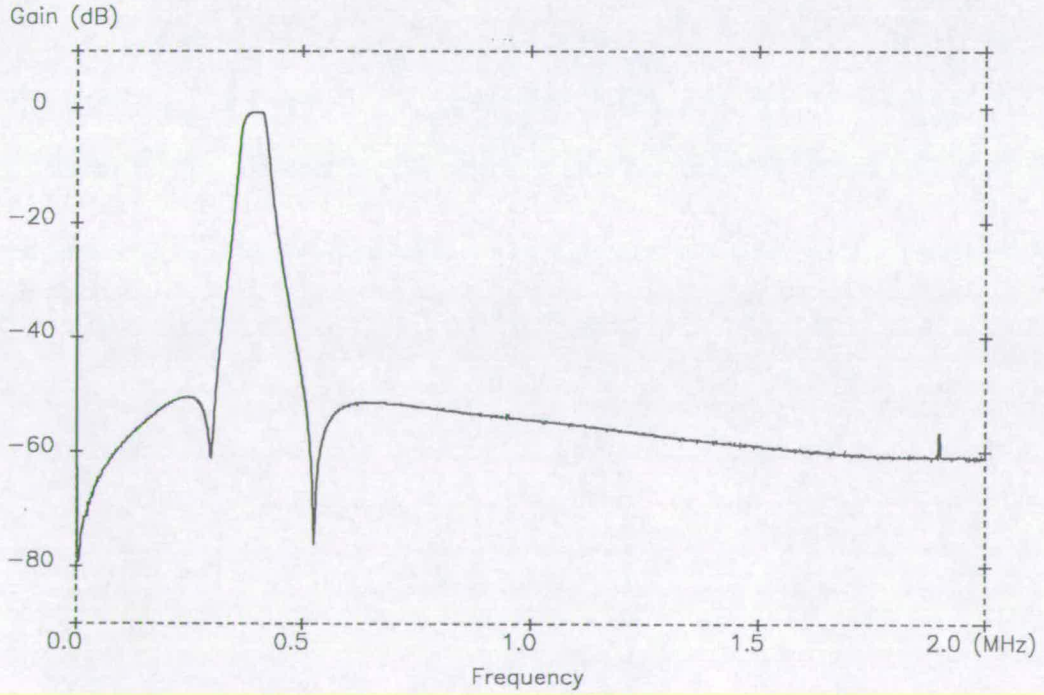


Figure 7.4-29 Measured amplitude response of BPF6

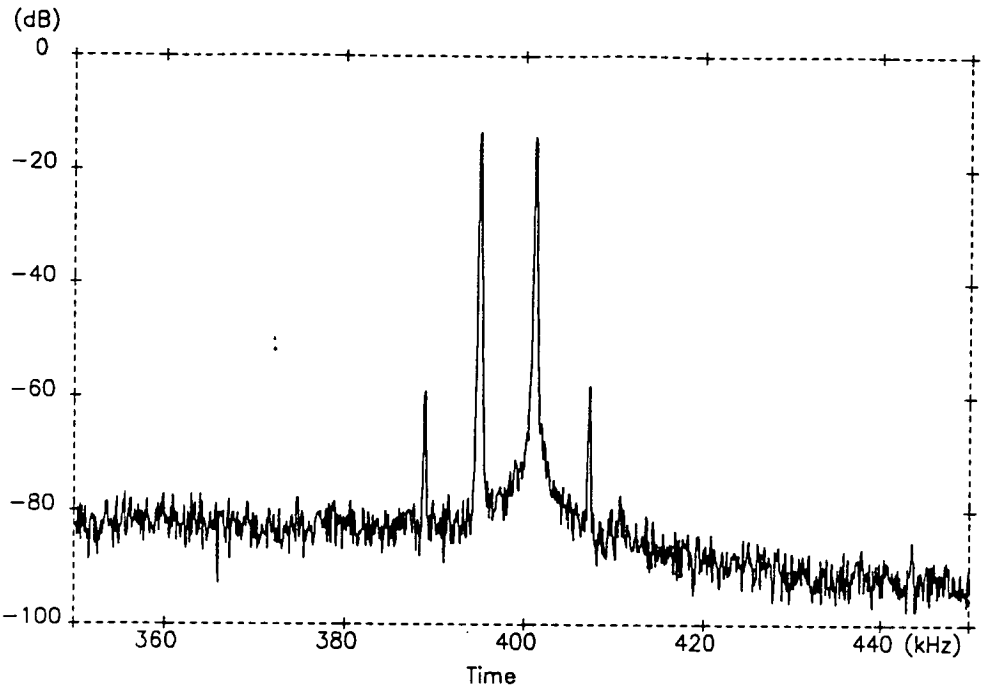


Figure 7.4-30 Spectrum of output of BPF6 used to determine intermodulation distortion. The two input terms are 100mV/395kHz and 100mV/401kHz

Parameter	Designed	Measured
centre frequency	400kHz	
tuning range of centre freq.		100kHz-525kHz
bandwidth	10%	10%
passband gain	0dB	-0.7dB
passband ripple	0.1dB	1dB
noise density in passband		920nV/$\sqrt{\text{Hz}}$
intermodulation distortion		-43.8dB
common mode rejection		72dB
cm to differential rejection		46dB
power supply rejection		40dB
current consumption	9.3mA	11.3mA

Table 7.4-7 Experimental results for BPF6

7.5 Control loop

The frequency control loop fabricated with the test filters is a phase lock loop based on a voltage controlled oscillator, as described in section 3.3. The only difference between the circuit shown in figure 3.3-3 and the fabricated circuit is that the former uses a harmonic oscillator and the latter a triangle wave oscillator. The relative merits of the two types of oscillator will be discussed in this section.

The principle of the triangle wave oscillator is illustrated in figure 7.5-1. An analogue switch selects either $+\Delta V$ or $-\Delta V$ as the input to the transconductor and respectively $+\Delta V/2$ or $-\Delta V/2$ as one of the inputs of the comparator. If $+\Delta V$ is selected then the voltage across the capacitor will slew up linearly at a rate $(\Delta Vg/C)$. When this voltage exceeds $\Delta V/2$, the comparator changes state so that the output of the analogue switch changes to $-\Delta V$. Then the output of the transconductor slews down until its value reaches $-\Delta V/2$ and the comparator changes state again. In each period the transconductor output has to slew twice through a range of magnitude ΔV, so the frequency of oscillation is:

$$f_{osc} = \frac{\Delta Vg/C}{2\Delta V} = \frac{g}{2C}. \qquad (7.5\text{-}1)$$

The output of the comparator is of course a square wave at the same frequency.

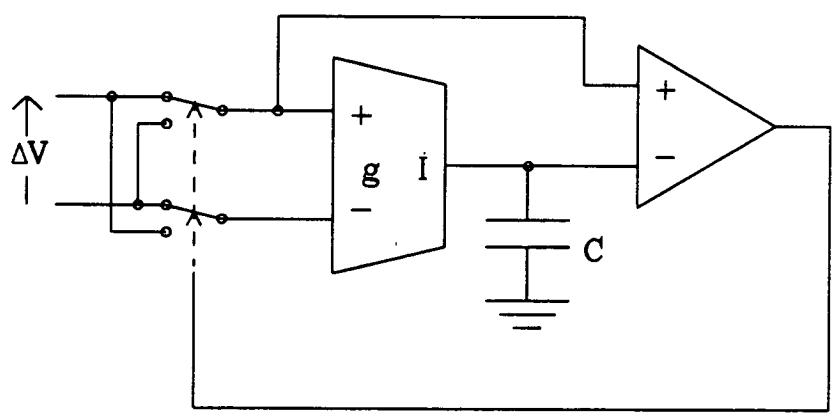


Figure 7.5-1 Triangle wave oscillator

The schematic of the on chip components of the control loop is shown in figure 7.5-2.

To complete the loop, an off chip single pole passive RC lowpass filter is connected between the port OUT and the input port VCIN.

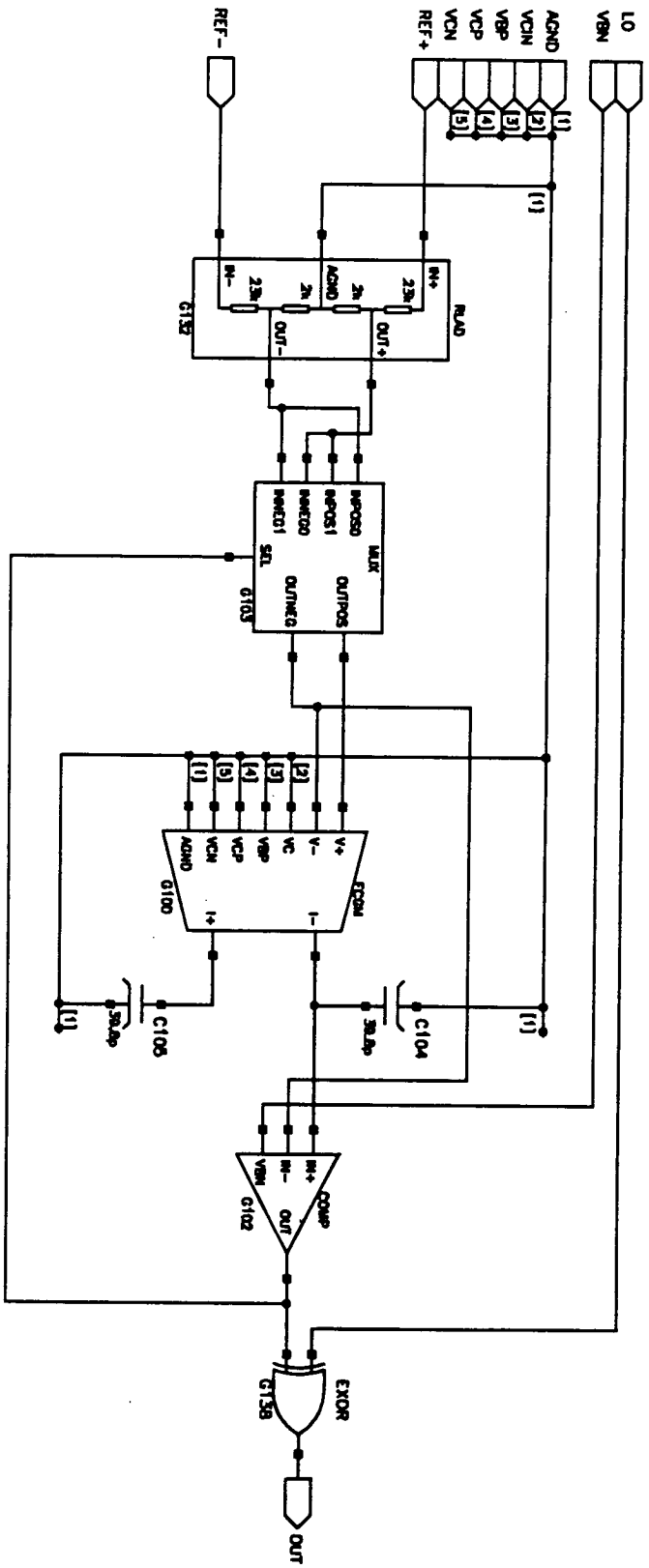


Figure 7.5-2 Schematic of frequency control loop using non-harmonic VCO

The ports VREF+ and VREF- are connected to VDD and VSS, so for a 5V supply the value of ΔV is 400mV. The block MUX passes either (INPOS0,INNEG0) or (INPOS1,INNEG1) according to the value of the digital input SEL (0 or 1 respectively). The value of the capacitors is chosen such that the transconductor should have a nominal value of 100μS for a reference clock of frequency (0.4π)MHz. Only C104 is in the signal path. C105 maintains the symmetry of the integrator in order to ensure common mode stability. The EXOR gate acts as a phase comparator between a square wave reference clock and the output of the VCO. The off chip RC loop filter extracts the d.c. control voltage from the square wave output of the EXOR gate. A change in the control voltage corresponds to a variation in the mark/space ratio of the EXOR output, which is effected by a shift in the phase difference between the reference clock and the VCO output.

The operation of the control loop is illustrated in figure 7.5-3 which shows the measured amplitude response of the filter BPF1 for three different values of clock frequency (844kHz, 944kHz and 1.044MHz). The centre frequencies of the responses are 355kHz, 400kHz and 445kHz respectively.

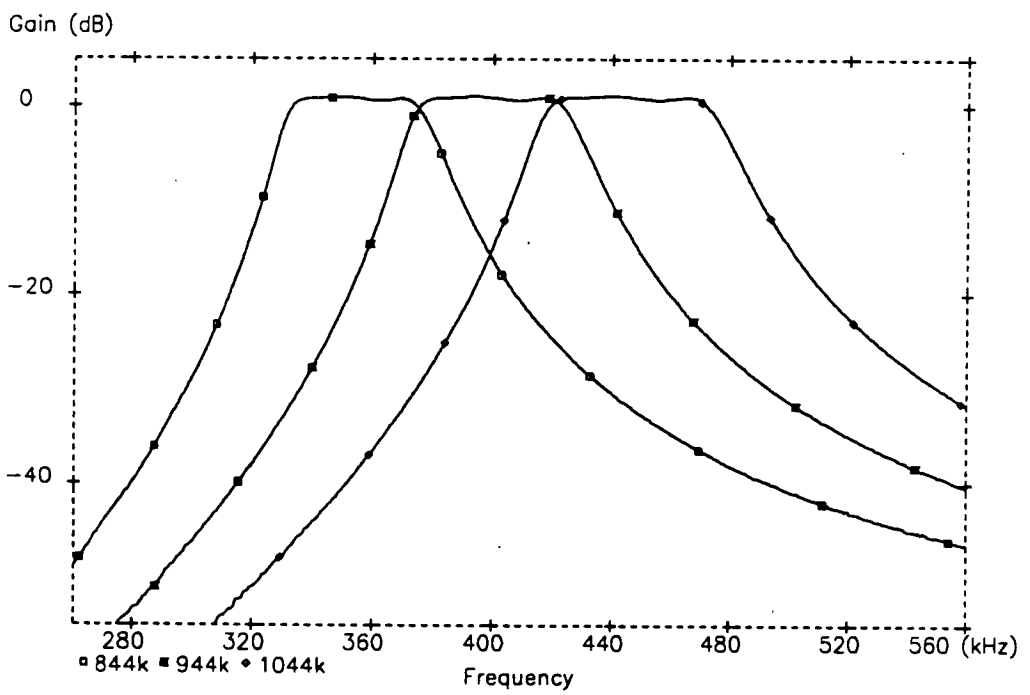


Figure 7.5-3 Amplitude response of BPF1 for three reference clock frequencies

Evidently a linear function exists as desired between the clock and centre frequencies, but this function has an offset and the wrong gain. For the centre frequency of 400kHz the clock/centre ratio has the value 2.36 when it should be π.

This represents an discrepancy of 33%. The most likely source of this error is the propagation delay of the comparator within the VCO. The effect this delay is to lower the frequency of oscillation for a given value of transconductance. The figures given above correspond to a propagation delay of 131ns. Some improvement upon this figure could be achieved by increasing the appropriate transistor aspect ratios and bias currents within the comparator, but the significant speed improvement that is obviously required is hard to obtain for two reasons. Firstly, the differential input voltage of the comparator at the moment it is meant to change state is zero by definition. Secondly, a strobed comparator (normally used for high speed applications) cannot be used here as the uncertainty in the time at which it is meant to act would imply an extremely high strobe frequency.

In general the following procedure is recommended to minimise the problem of propagation delay in the triangular wave VCO: 1. Choose as low a reference frequency as possible. This is obviously easier for bandpass filters since the reference can then be placed within the lower stopband. 2. Design as fast a comparator as possible, subject to the limitation of available bias current. 3. Compensate for the effect of the comparator propagation delay by reducing the values of the load capacitors in the VCO, using a simulator to converge upon the optimum value.

The problem described above does not occur if a harmonic VCO is used. At the time of designing the test chips the non-harmonic oscillator was preferred due to the problem of controlling signal amplitudes in the harmonic VCO. The optimum solution may be to use a harmonic VCO with amplitude dependent load impedances [30] or an amplitude lock loop (section 3.4).

A photomicrograph of the fabricated control loop is shown in figure 7.5-4.

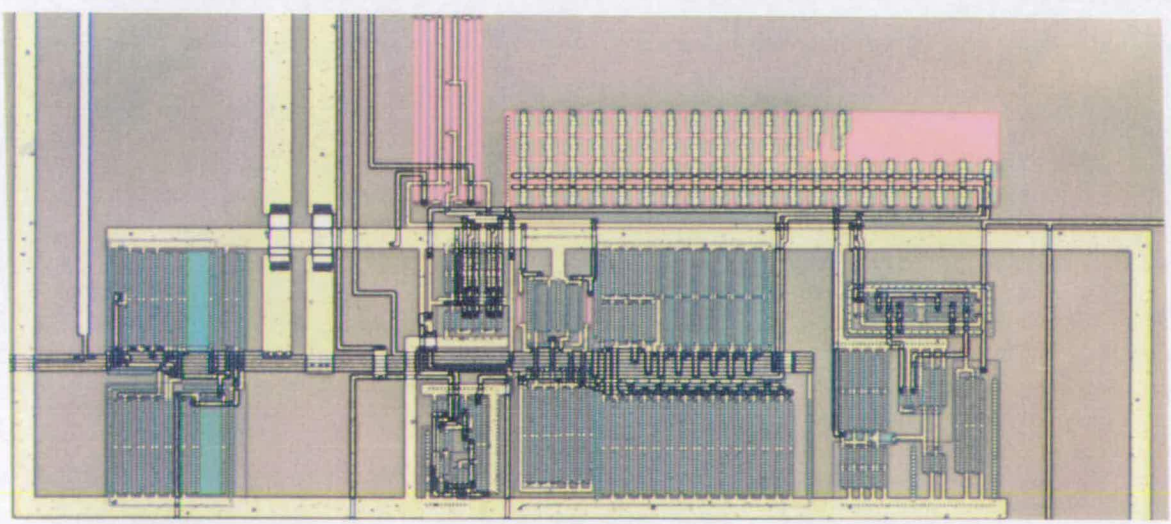


Figure 7.5-4 Photomicrograph of the control loop

7.6 Output buffer

Since the output impedance of a transconductor filter is moderately high (approximately equal to the reciprocal of the terminating transconductance) unity gain buffers must be used to drive the output signals off chip. For filters with passbands in the region of 1MHz the design of an output buffer is challenging, because the gain of the buffer must be as high as possible at the signal frequencies. If this condition is not met then the amplitude of the differential input voltage of the buffer will be a significant fraction of the signal amplitude, and harmonic distortion will be introduced. As a general rule, the unity gain frequency of the buffer should be at least an order of magnitude greater than the upper passband frequency of the filter in question.

The circuit of the buffer amplifier designed for the test chips is shown in figure 7.6-1. The topology of this circuit is similar to that of the standard 7 transistor CMOS amplifier, the difference being that the load of the output stage MN5 is biassed not by a d.c. source but by the current in the input stage load MP6 via a current amplifier [56]. The output of the amplifier can therefore be considered of class AB, though it should be noted that the output is not symmetrical since there are two stages of voltage gain to the output through MP9 but only one through MN5. The amplifier is provided with standard Miller compensation by Rz and Cc. To form a unity gain buffer, the output is connected to the negative input.

It is important that the buffer present as small a load as possible to the filter. For this reason an n-type input stage is used since this gives a particular gain with a smaller aspect ratio than would a p-type input. For frequencies well within the bandwidth of the amplifier, the load capacitance seen by the filter is less than the gate capacitance of the input transistor MN2 since the negative feedback of the unity gain buffer forces all the a.c. signals in the differential stage to follow the input signal.

Figure 6.7-2 shows the simulated gain and phase of the open loop buffer amplifier with a load of 100kΩ in parallel with 100pF. The unity gain frequency is 16.8MHz, the phase margin is 58^{o} and the gain margin is 20.4dB. Experimental results for the buffer amplifier alone are not available, however from the results given in sections 7.2 to 7.5 its operation is clearly satisfactory.

Figure 7.6-3 is a photomicrograph of the buffer amplifier situated in the padring of one of the test chips.

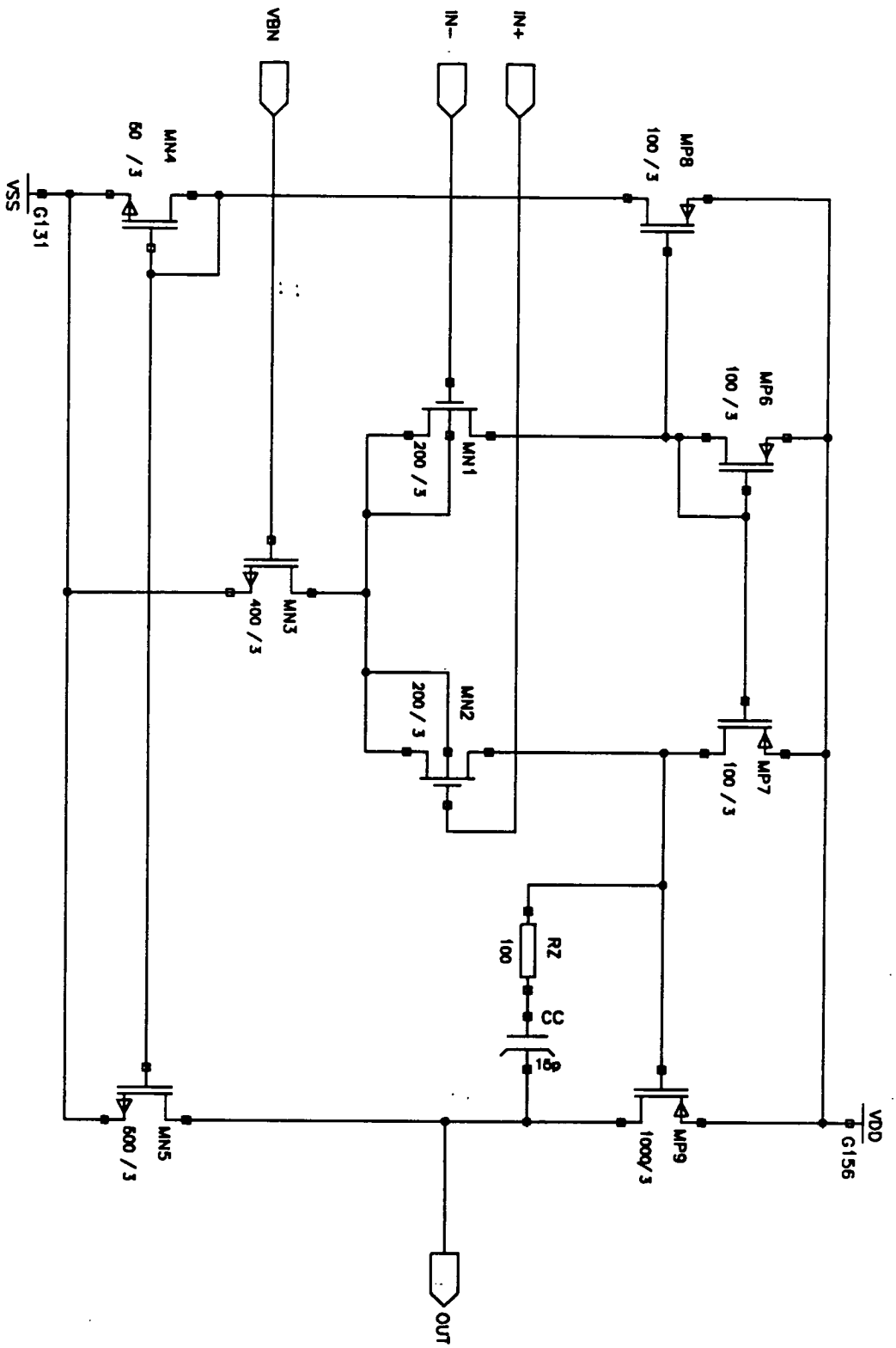


Figure 7.6-1 Schematic of output buffer

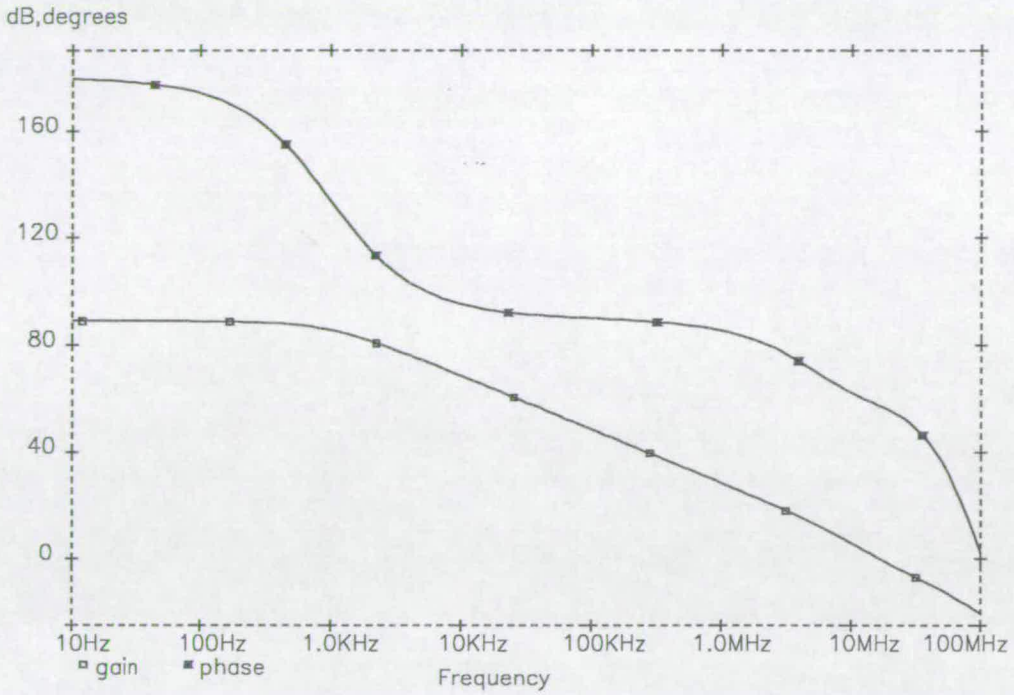


Figure 7.6-2 Simulated open loop gain and phase of buffer amplifier for 100pF/100kΩ load

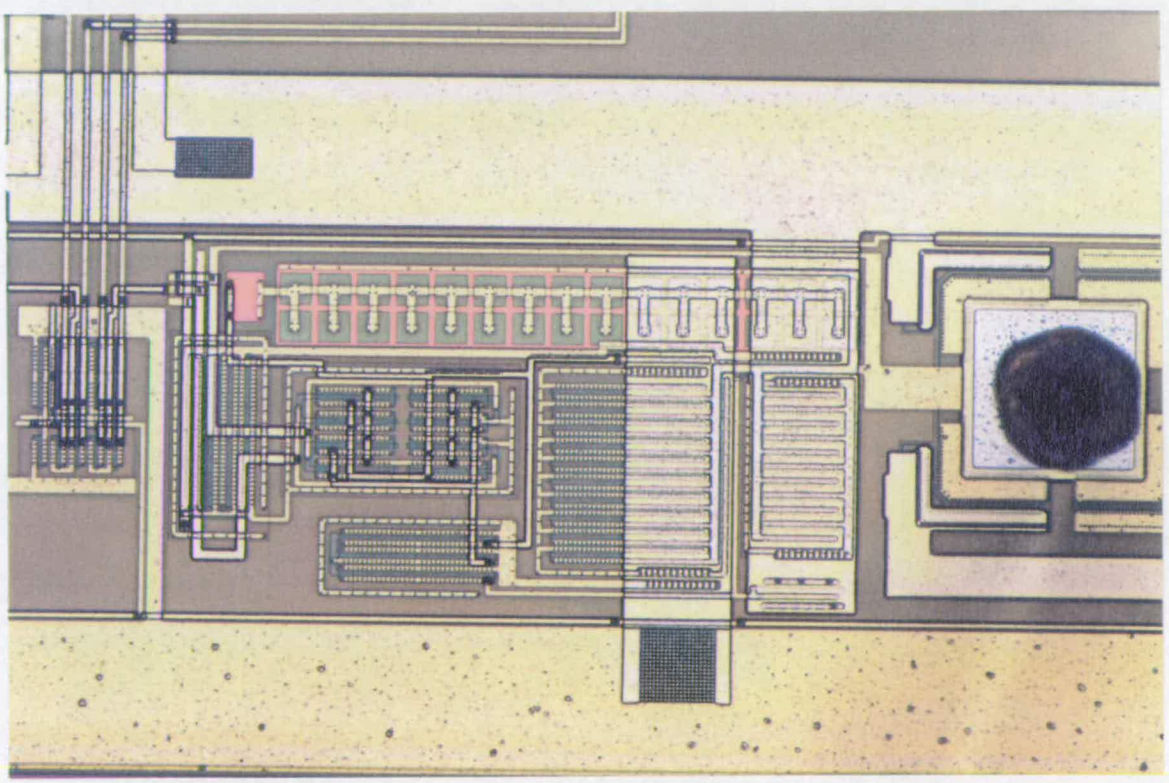


Figure 7.6-3 Photomicrograph of buffer amplifier in padring of test chip

CHAPTER 8
CONCLUSIONS

Finally we review the most important developments described in the previous chapters and make suggestions for further research.

A new CMOS circuit (the "grounded quad") for linear tunable voltage to current conversion is introduced in chapter 4. The advantages of this circuit are that it can operate easily in a low voltage process and that it is very simple, requiring only four transistors for the transconductance function. It has a linearity (≅60dB for signals around 150mVrms) that is sufficient for common high frequency filtering applications such as video signal processing. A simple transfer function for the grounded quad is developed. This analysis could be extended to gain further insight into how to choose the transistor aspect ratios for best linearity.

The advantages of folded cascode circuits as transconductors are demonstrated by analysis and example, and two enhancements to the standard folded cascode structure are introduced in chapter 5. The first is the inclusion of low impedance inputs in the transconductor, which allows the design of original types of ladder filter using matrix methods. The second is a circuit which can compensate actively for phase errors in the transconductor. The most immediate continuation of this work should be experimental verification of the phase correction technique by the design and fabrication of a vector lock loop.

Matrix based methods for the design of transconductor ladder filters are presented in chapter 6. Each type of response is considered in turn, from lowpass to allpass. The matrix methods are most successful for bandpass filter design: the Right Inverse decomposition allows any response to be realised using only two values of conventional transconductor. When transconductors with low impedance inputs are available, the Left Inverse decompositions allow any bandpass response to be realised using a single value of transconductance. If the response is symmetric, the Left Inverse (type 2) decomposition can be used to obtain the simplest filter structure. For all-pole bandpass filters the Left Direct decomposition is usually best. A very important continuation of this work is to investigate the sensitivities of the new filter structures to component tolerances. This sensitivity is not easy to predict since the passive components in a filter designed with an inverse matrix decomposition do not correspond individually to components in the passive prototype. Another opportunity for further work is the investigation of asymmetric passive prototypes whose matrices

remain sparse even after inversion.

The experimental filters described in chapter 7 give results better than most to be found in the literature. The only disappointing observation is that although the frequency control loop is functionally correct, the ratio between the reference and filter centre frequencies is not. The reasons for and solutions to this problem are discussed in chapter 7. Further work should include improving the performance of the control loop, and trying out those decompositions (such as LI type 2) which were discovered after the submission of the test chips to fabrication.

APPENDIX A
PHASE ERRORS IN TRANSCONDUCTOR FILTERS

The gain and phase of an ideal integrator with 1 Hz unity gain frequency are illustrated in figure A-1. The phase shift is exactly -90° at all frequencies.

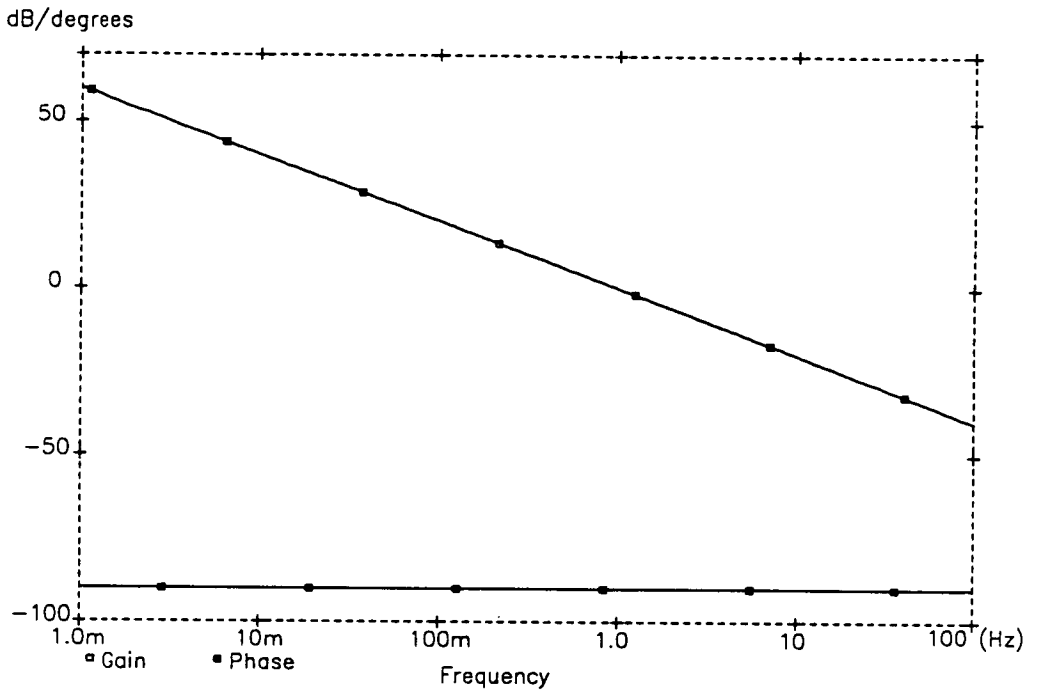


Figure A-1 Gain and phase of ideal integrator as a function of frequency

Filters constructed from integrators are very sensitive within the passband to departures from this ideal integrator phase response. The purpose of this appendix is to illustrate the sources of phase errors in transconductors and their effect upon filter amplitude responses. Additional discussion of this subject is given in section 5.4 where the principle of a technique for the active cancellation of phase errors is introduced.

Phase lead is the term used to describe an integrator phase shift of magnitude less than 90° (i.e. $\phi > -90^{o}$). This is tends to be caused by the finite output impedance of the transconductor in the integrator. Figure A-2 shows the gain and phase plot of an integrator whose transconductor has an output conductance equal to one hundredth of its transconductance (i.e. its d.c. gain is 100). At the unity gain frequency the phase shift is -89.47°.

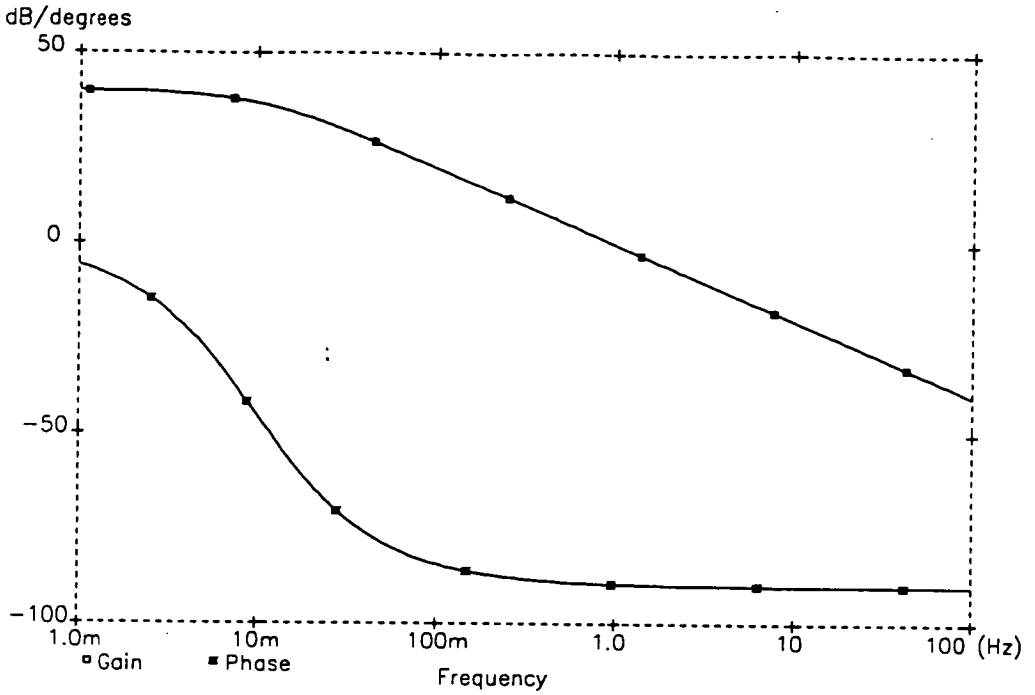


Figure A-2 Gain and phase of transconductor integrator with finite output impedance

Phase lag or *excess phase* refers to an integrator phase shift of magnitude greater than 90^{o} (i.e. $\phi<-90^{o}$). This tends to be caused by parasitic poles associated with any parasitic capacitance in the transconductor. Figure A-3 shows the gain and phase plot of an integrator whose transconductor has a non-dominant pole at one hundred times the frequency of the dominant pole. At the unity gain frequency the phase shift is -90.57^{o}.

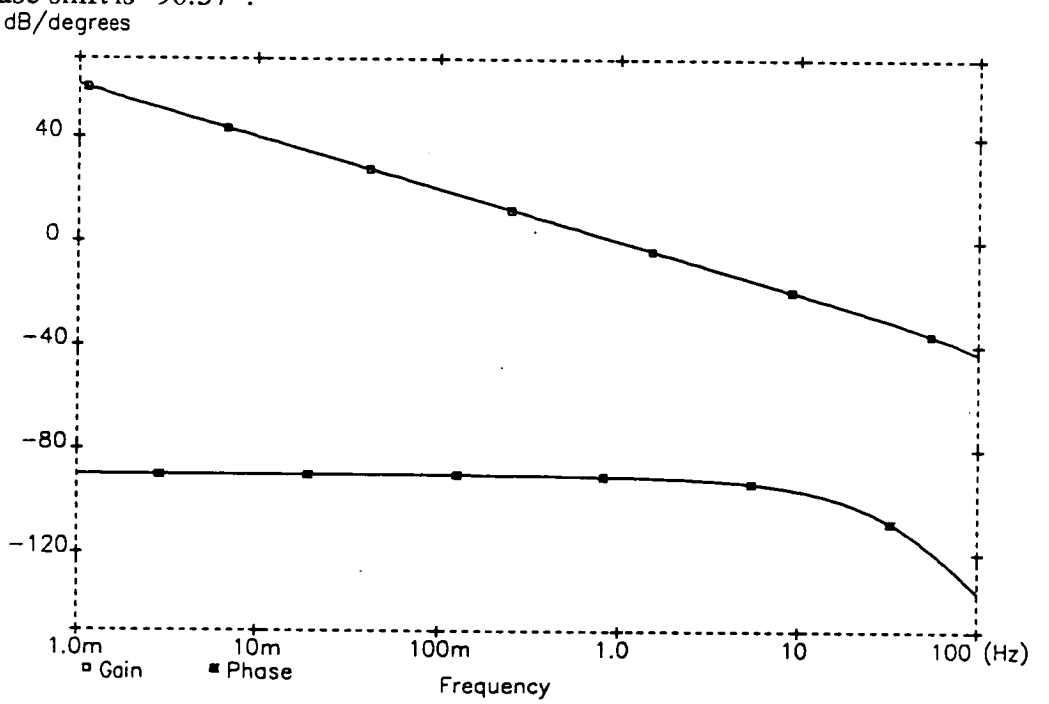


Figure A-3 Gain and phase of transconductor integrator with one non-dominant pole

The gain and phase of a more typical transconductor are shown in figure A-4. In this case the effects of finite gain and of a non-dominant pole can both be seen.

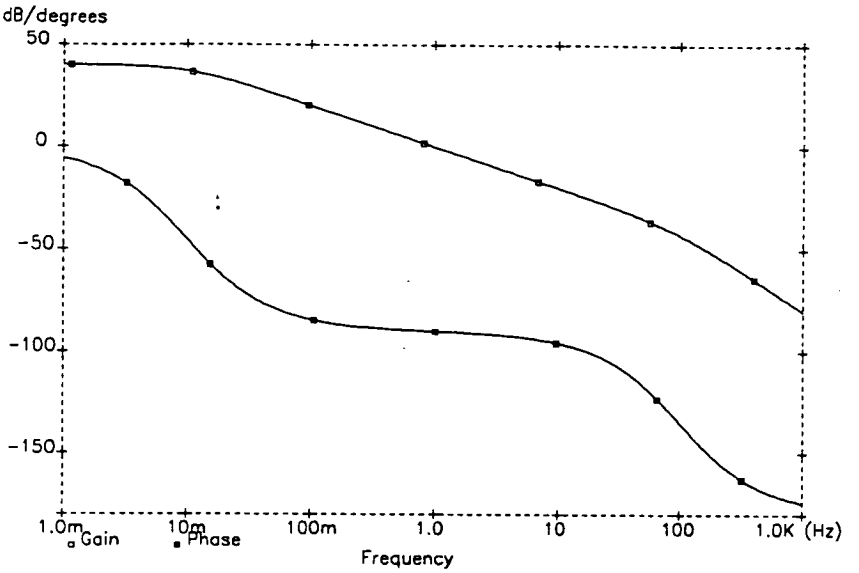


Figure A-4 Gain and phase of transconductor integrator with finite output impedance and a parasitic pole

The effects of phase errors on a filter depend upon the class, order and selectivity of its transfer function. The simplest way to investigate these effects are to simulate the filter using a macromodel for the transconductor such as that shown in figure A-5. The first stage of this has unity d.c. voltage gain, and a pole at angular frequency g/Cp which simulates the cumulative effect of parasitic poles in a real transconductor. The second stage simulates the nominal transconductance g and the output impedance Zout.

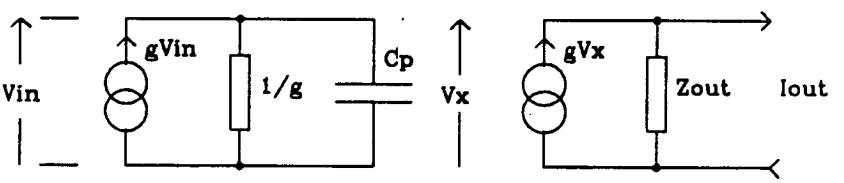


Figure A-5

Macromodel of transconductor with finite output impedance and one parasitic pole

When the macromodel is used to simulate the sixth order Chebyshev bandpass filter, the results shown in the following two figures are obtained. The schematic of the filter is that shown in figure 3.2-23, renormalised to a centre frequency of 1Hz.

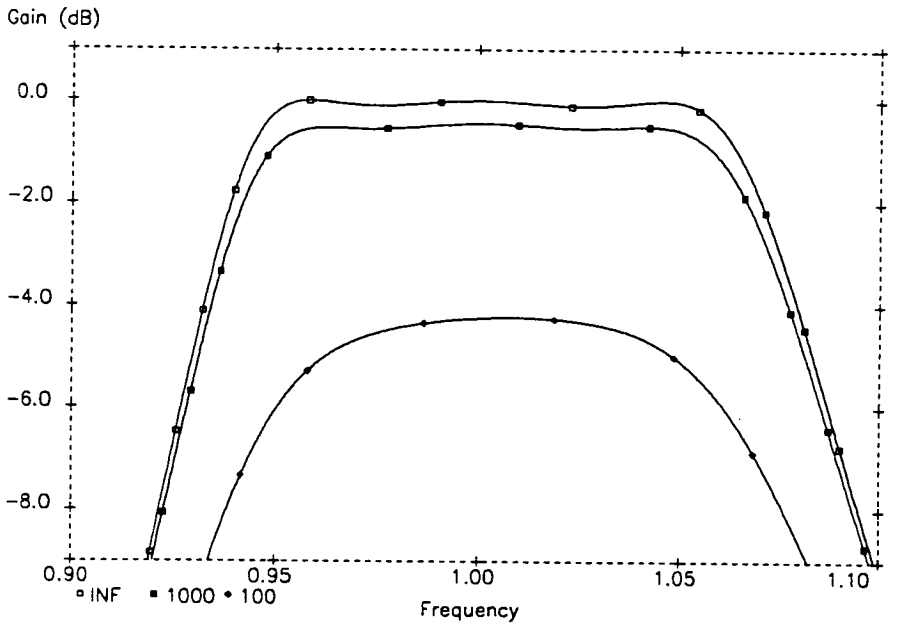


Figure A-6 Magnitude response of bandpass filter with three values of transconductor voltage gain: infinite, 1000 and 100

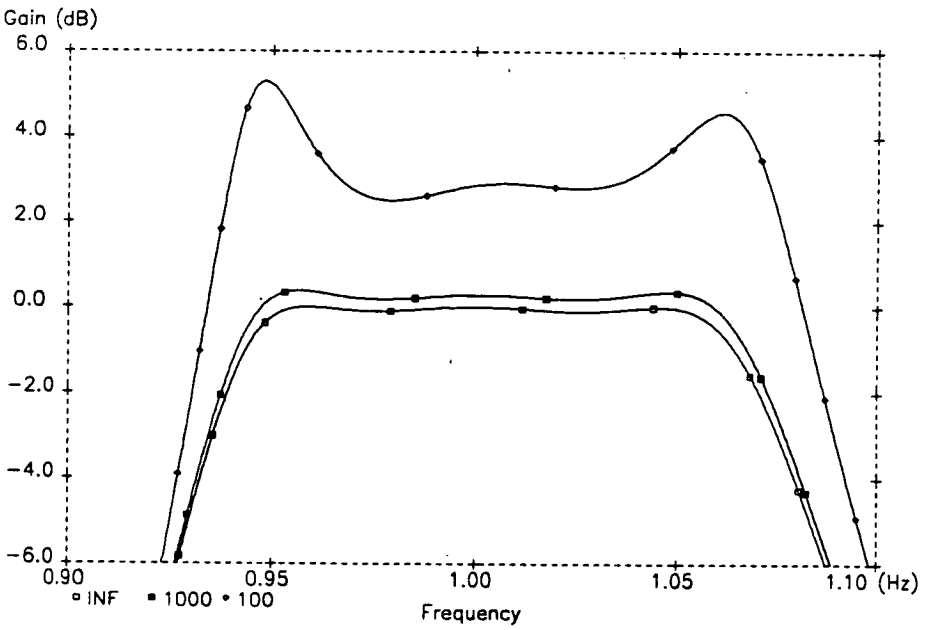


Figure A-7 Magnitude response of bandpass filter with three values of transconductor parasitic pole frequency: infinite, 1000 times centre freq. and 100 times centre freq.

The result of low transconductor output impedance is droop in the passband amplitude response. Figure A-6 shows the ideal response and the response with two finite values of transconductor output impedance. With a transconductor voltage gain of 1000 the response retains its shape, but has a loss of about 0.5dB. With a transconductor voltage gain of 100 there is an attenuation of over 4dB at the centre frequency and the shape is severely distorted.

The effects of excess phase on the bandpass filter response are shown in figure A-7. In this case gain increases within the passband, particularly at the edges; an effect known as Q-enhancement. When the parasitic pole in each transconductor is 1000 times the centre frequency the passband gain is approximately 0.3dB. When the parasitic pole frequency is only 100 times the centre frequency, the gain is over 2dB and the passband shape is severely distorted. A filter suffering from severe Q-enhancement could be expected to oscillate.

The corresponding results for a lowpass filter are shown in the following two figures. This filter has a fifth order Butterworth response. The schematic is figure 6.2-5, rescaled to a -3dB frequency of 1Hz. Qualitatively, the effects of phase lead and lag are the same as for the bandpass filter, i.e. droop and peaking respectively in the passband. However the distortion is much less severe in this case. In general, sensitivity to phase errors increases with filter selectivity. So it is greatest for narrow bandpass filters.

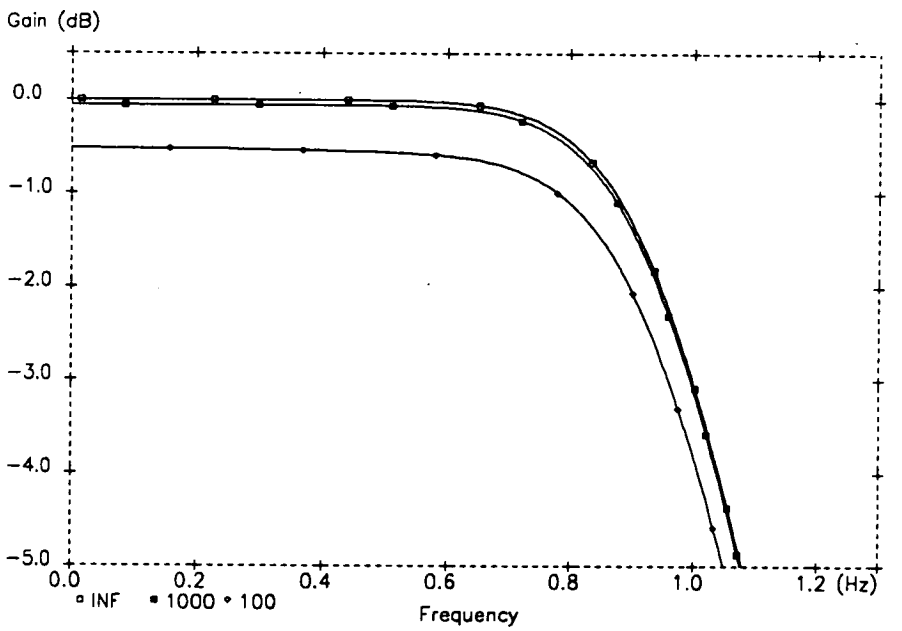


Figure A-8 Magnitude response of lowpass filter with three values of transconductor voltage gain: infinite, 1000 and 100

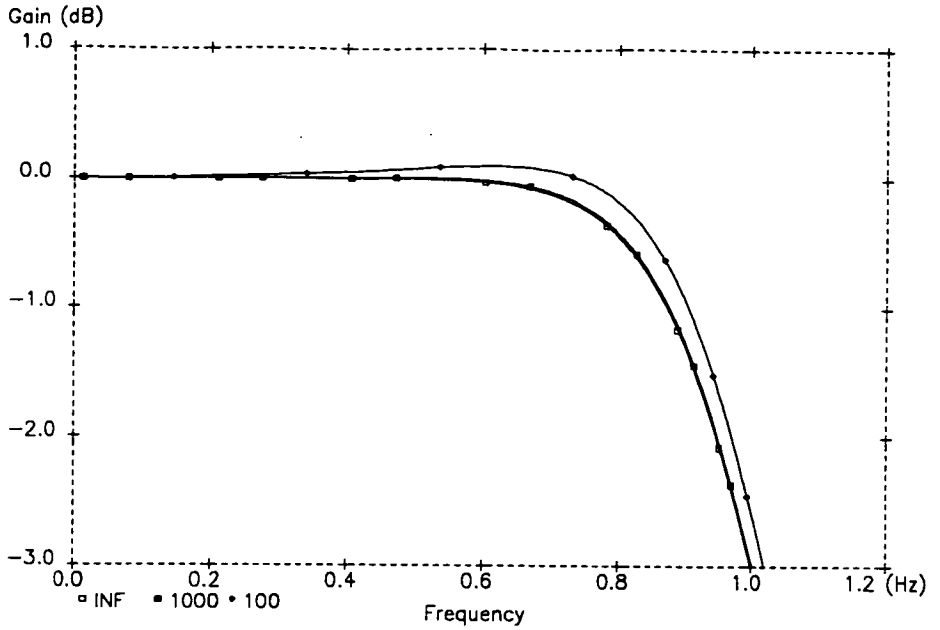


Figure A-9 Magnitude response of lowpass filter with three values of transconductor parasitic pole frequency: infinite, 1000 times centre freq. and 100 times centre freq.

In this appendix only all-pole filters have been simulated. It should be noted that the polarity of the phase distortion for elliptic filters depends on the particular response concerned.

APPENDIX B
TRANSISTOR MODEL EQUATIONS

A summary of the simple transistor equations used for the calculation of circuit properties in the course of the thesis. The derivations of these equations can be found in standard texts [5,15,25,29,56]. It should be emphasised that more sophisticated models are used in computer simulation programs [22]. The symbols used here are defined on pages iii to v.

The MOS Transistor

Two modes of operation are defined: *triode* (or *linear*) mode in which

$$V_{ds} < V_{gs}-V_t \tag{B-1}$$

and *saturation* mode in which

$$V_{ds} > V_{gs}-V_t. \tag{B-2}$$

Care should be taken to avoid confusion with the terms 'saturation' and 'linear' applied to bipolar transistors, since saturation then refers to the *lower* range of output (i.e. collector-emitter) voltage.

In saturation mode the MOSFET channel current is given by

$$I_{ds} = \beta(V_{gs}-V_t)^2 \tag{B-3}$$

where

$$\beta = \frac{W}{L}K'. \tag{B-4}$$

Simple theory predicts a value for K' equal to the product of the carrier mobility in the channel and the gate capacitance per unit area.

The transconductance of the saturated MOSFET is

$$gm = \frac{\delta I_{ds}}{\delta V_{gs}} \equiv \sqrt{2\beta I_{ds}}. \tag{B-5}$$

The output impedance is given by

$$gds = \frac{\delta I_{ds}}{\delta V_{ds}} \cong \lambda I_{ds} \tag{B-6}$$

The "channel length modulation factor" λ is given for small values of L by

$$\lambda = \frac{\theta}{L} \tag{B-7}$$

where θ is an empirical parameter. So the nominal voltage gain of a MOSFET is

$$A = \frac{gm}{gds} \cong \sqrt{\frac{2K'WL}{\theta^2 I_{ds}}}. \tag{B-8}$$

The channel current of a MOSFET in triode mode is given by

$$I_{ds} = \beta[(V_{gs}-V_t)V_{ds} - \left[\frac{1+\delta}{2}\right]V_{ds}^2] \tag{B-9}$$

Usually δ takes the value 0 in elementary treatments.

Bipolar Transistors

The collector current is given by

$$I_C = I_S \exp\left[\frac{V_{be}}{V_T}\right] \tag{B-10}$$

where

$$V_T = \frac{kT}{q}. \tag{B-11}$$

The transconductance is given by

$$gm = \frac{I_C}{V_T}. \tag{B-12}$$

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The following publications of the author are bound with this thesis:

Greer N.P.J., and Denyer P.B., "New folded cascode transconductor for bandpass ladders", IEE Proc. Pt G, vol. 138 no. 5, pp. 551-556, Oct. 1991

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New folded cascode transconductor for bandpass ladder filters

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Indexing terms: Circuit theory and design, Filters and filtering

Abstract: The problems of designing CMOS transconductors for high frequency bandpass ladder filters are discussed, and an original circuit for overcoming these problems is presented. This circuit features a new grounded-quad input stage, a very high output impedance and the facility of low impedance inputs to avoid the requirement for transconductance ratios in scaled filters. The application of the new transconductor is illustrated by the design of a high frequency sixth-order Chebyshev bandpass filter. The performance of the transconductor and the filter are demonstrated by analysis and simulation results.

1 Introduction

Considerable effort has been directed toward the development of linear transconductors for the implementation of integrated CMOS continuous time filters [1–7]. A number of circuits proposed have been based on the long tail pair linearised by means of source degeneration [1, 2] or crosscoupling [3]. Such circuits have good linearity and because of the simplicity of their structure, they do not suffer greatly from nondominant poles associated with parasitic capacitances. However, when designing bandpass filters, it is found that single stage transconductors of this type are unsatisfactory in several respects.

The maximum voltage gain that can be obtained from a single CMOS stage is around 35 dB owing to the relatively low output impedance. In a typical bandpass filter the phase lead caused by this low impedance results in severe distortion of the passband response. Khorramabadi and Gray [3] attempted to solve this problem by designing device sizes such that the phase lead was cancelled by the phase lag of the nondominant poles. In practice this solution is not practical because of the requirements that process parameters such as the channel length modulation factor be known precisely and remain constant, and that the transconductor be redesigned for each new frequency of application. A better solution is to adopt a cascaded biquad filter structure regulated by means of quality factor control loops [4]. Such circuits are expensive in terms of silicon area and power consumption. So for filters with centre frequencies up to around 1 MHz the best approach is to adopt a ladder structure based on transconductors with very high output impedance.

The second drawback of using single stage transconductors in a bandpass ladder filter is that transconductance ratios are required to scale correctly the nodal voltages of the filter. This scaling is essential not only to maximise the dynamic range but to prevent the integrators from having unity gain frequencies above the filter passband, which would be more susceptible to the effects of parasitic poles. The ratio of transconductances required is typically equal to the Q-factor of the filter. This implies that for a filter of moderate to high Q-factor transconductors have to be used with either very small input devices which are liable to match poorly or very large input devices which require high bias currents and have large parasitic capacitances. By careful choice of a passive prototype the use of the smaller transconductance can be limited to the simulation of the termination resistors which are considerably less sensitive to imperfection than the reactive components. The requirement remains that the transconductor has to be modified each time a different filter is designed.

The voltage swing of a single CMOS stage in the region of the unity gain frequency is limited to approximately one threshold voltage (i.e < 1 V) as signals greater than this will turn the input devices into triode mode, causing severe distortion. This point applies equally to low pass filters.

All three problems described can be solved by the use of folded cascode (FC) transconductors. Such circuits are linearised versions of the folded cascode operational transconductance amplifiers (OTAs) used routinely in switched capacitor circuits [5], and occasionally used in continuous time filters [6]. The linearisation can be achieved by the same techniques as those used for single stage transconductors but without the accompanying dynamic range limitations, since the output is no longer taken from the drains of the input devices. The cascode structure provides a very high output impedance. Equally importantly, an FC transconductor can be given low impedance input nodes (in addition to the standard high impedance inputs) thus circumventing the need for ratioed input transistors when the circuit is used in a bandpass ladder filter.

In this paper a new grounded quad transconductance cell is introduced, the advantages of low impedance inputs are discussed and an original FC transconductor circuit is presented which includes both features. The application of the new circuit is illustrated by the design of a high frequency Chebyshev bandpass ladder filter.

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2 Grounded quad transconductance cell

The new MOS transconductance cell is illustrated in Fig. 1. It consists of two input devices operating in saturation mode, each of which is degenerated with respect to the negative supply by the channel conductance of another transistor operating in triode mode. The input voltage is

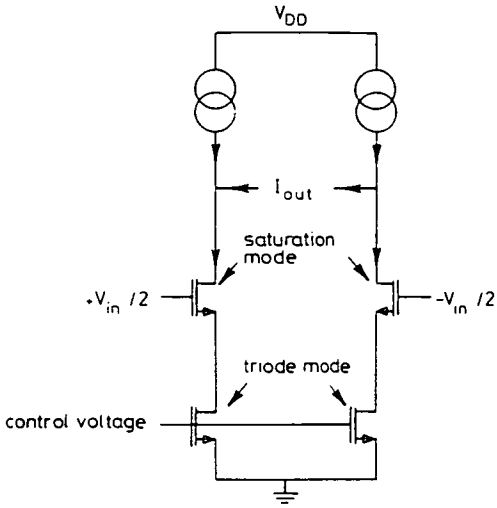

Fig. 1 *Grounded quad transconductance cell*

differentially applied to the gates of the saturation mode devices and the output current is taken as the difference between the two currents produced. The transconductance of the quad is controlled by the voltage applied to the gates of the triode mode devices, which adjusts their channel conductance.

To develop a transfer function for the grounded quad cell, we make the simplifying assumptions that, for a particular control voltage the channel resistance of each triode mode device has a constant value R and that the body effect can be neglected. The current in one side to the quad is first found. Into the standard equation

$$I = 0.5\beta(V_{gs} - V_t)^2 \tag{1}$$

for the current in a saturated MOSFET (where the symbols have their usual meanings) we make the substitution

$$V_{gs} - V_t = V_{in}/2 + V_o - IR \tag{2}$$

where V_{in} is the differential input voltage, V_o is the difference between the signal ground with respect to the negative supply rail and the threshold voltage, and IR is the voltage across the channel of the triode mode device. The resulting quadratic equation is solved to obtain

$$I = [1 + \beta RV_o + \beta RV_{in}/2 - \sqrt{(1 + 2\beta RV_o + \beta RV_{in})}]/\beta R^2 \tag{3}$$

The current in the other side of the cell is given by an equation identical to eqn. 3 but with $V_{in}/2$ replaced by $-V_{in}/2$. The difference between these two currents is used to obtain the output current

$$I_{out} = (V_{in}/R) - (c/\beta R^2) \times [\sqrt{(1 + \beta RV_{in}/c^2)} - \sqrt{(1 - \beta RV_{in}/c^2)}] \tag{4}$$

where

$$c = \sqrt{(1 + 2\beta RV_o)} \tag{5}$$

Eqn. 4 is simplified by expanding the square roots and retaining terms up to the third harmonic:

$$I_{out} = (V_{in}/R)(1 - c^{-1}) - (R\beta^2/8c^5)V_{in}^3 \tag{6}$$

It is clear from eqn. 6 that the most linear behaviour is obtained when the transconductance of the saturation devices is much greater than the channel conductance of the triode devices; the product βR and the term c then tend to large values, so that the third harmonic is deemphasized and the overall transconductance tends to $1/R$. This limit, which is intuitively obvious, corresponds to the differential input voltage simply being level-shifted onto the drains of the triode devices. Unfortunately the limit cannot be exploited too far, as making the saturation devices wide burdens the transconductor with a large input capacitance and making the triode devices too small is detrimental to matching. However, even when all the devices in the quad cell are of similar dimensions, the third harmonic of eqn. 6 is very small, as is confirmed by our simulation results.

Since the transconductance is a function of the common mode level of the input signal, care should be taken with power supply decoupling and with the common mode feedback of the circuit from which the input is taken (usually another identical transconductor).

In addition to its linearity, the grounded quad cell is attractive for its simplicity, and the absence of saturation mode devices in series makes it particularly suitable for use in low voltage processes.

3 Low impedance transconductor inputs

Traditionally, the building block used to synthesise transconductor-C filters has been the integrator with summing inputs (Fig. 2) whose transfer function is

$$V_{out} = \left(\sum_i g_i V_i\right) \Big/ sC \tag{7}$$

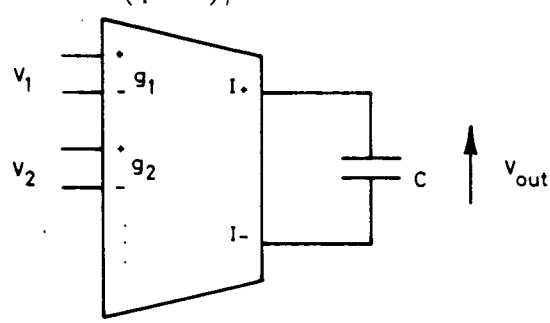

Fig. 2 *Transconductor-C integrator with summing inputs*

where C is the value of the integration capacitor, V_i are the input voltages and g_i is the transconductance of the ith input. A multi-input transcondcutor can be implemented as a single circuit with different input stages connected in parallel or as separate transconductors with their current outputs connected together. In most cases the only real difference between these two implementations is the way the schematic diagrams are drawn. The distinction sometimes made [1] between direct filter synthesis (using gyrators) and indirect, based on signal flow graphs, is usually trivial for the same reason.

The use of eqn. 7 to synthesise bandpass ladder filters is unsatisfactory because correct nodal scaling forces widely differing values of g_i to be used. As well as impairing the performance of the circuit this means that the transconductors in a filter design system cannot be standardised, since each new filter specification may imply a different optimum transconductance ratio. A much more flexible building block transfer function is

$$V_{out} = \left(gV_1 + s\sum_i C_i V_i\right) \Big/ sC \tag{8}$$

This is realised, as before, by a transconductor with a load capacitor, but now the current output of the transconductor is the sum of the current from a conventional

input (of transconductance g) and that from an arbitrary number of capacitors of value C_i connected between input voltages V_i and a low impedance current summing input to the transconductor. This new first-order building block is shown in Fig. 3, where we use $Z+$ and $Z-$ to denote the low impedance inputs of the transconductor.

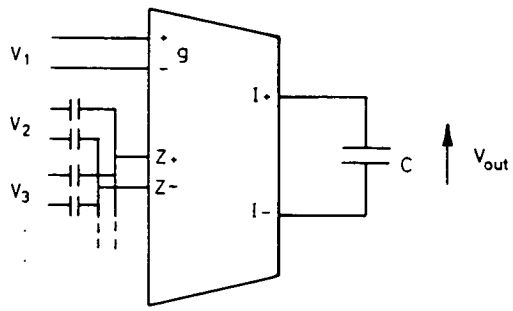

Fig. 3 *New first order transconductor-C building block*

The nonintegrating terms of the building block can also be implemented by connecting capacitors directly between the input nodes and the integration capacitor. Such capacitors can usually represent only bidirectional coupling paths since both plates will normally be connected to integrator outputs which are of high impedance. The only common exception to this is the input capacitor, assuming that the filter is driven by a low impedance voltage source. When a capacitor is used to implement a unidirectional coupling path driven by an internal node, low impedance transconductor inputs represent the only feasible solution. In principle, a capacitor could also be made unidirectional by driving one of its plates with a voltage buffer. In practice, it is found that even the simplest voltage follower introduces sufficient phase shift to severely distort a filter passband.

It should be noted that eqn. 8 is only valid when the impedance of the capacitors is much less than the output impedance of the transconductors, and so although this building block is ideal for bandpass filters it would not be suitable for lowpass filter design.

4 New folded cascode transconductor

The new folded cascode transconductor based on the grounded quad cell is shown in Fig. 4. A p-type input is used since this requires larger devices (for a given transconductance), which improves matching between transconductors. The inclusion of low impedance inputs is very simple: the nodes used are the drains of the current sink transistors about which the circuit is folded (M5 and M12), and the low impedance is achieved by biasing the gates of the adjacent cascode devices (M6 and M13) not from a fixed voltage but from the outputs of single stage inverter-amplifiers (M9–M11 and M16–M18) whose inputs are the respective low impedance nodes. The same structure has been used elsewhere to obtain improved cascode output impedance [9]. A similar technique has also been used in a triode mode CMOS transconductor [7] to hold the drain voltages of the input transistors constant and to provide a means of nulling the effect of capacitor bottom plate parasitics. Common-mode stability is provided by the circuit shown in Fig. 5

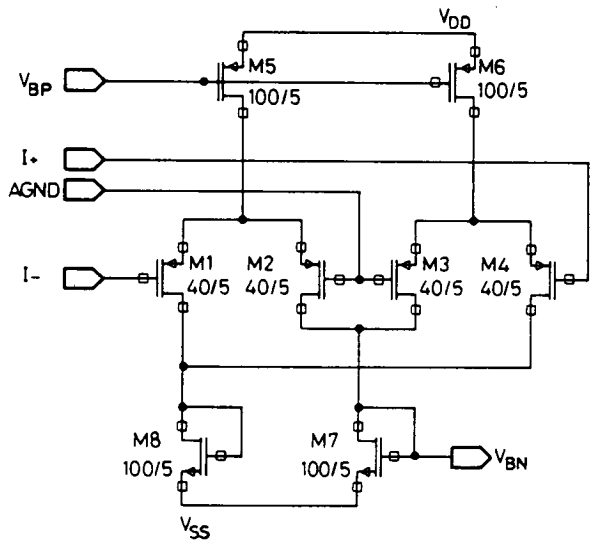

Fig. 5 *Common-mode feedback circuit*

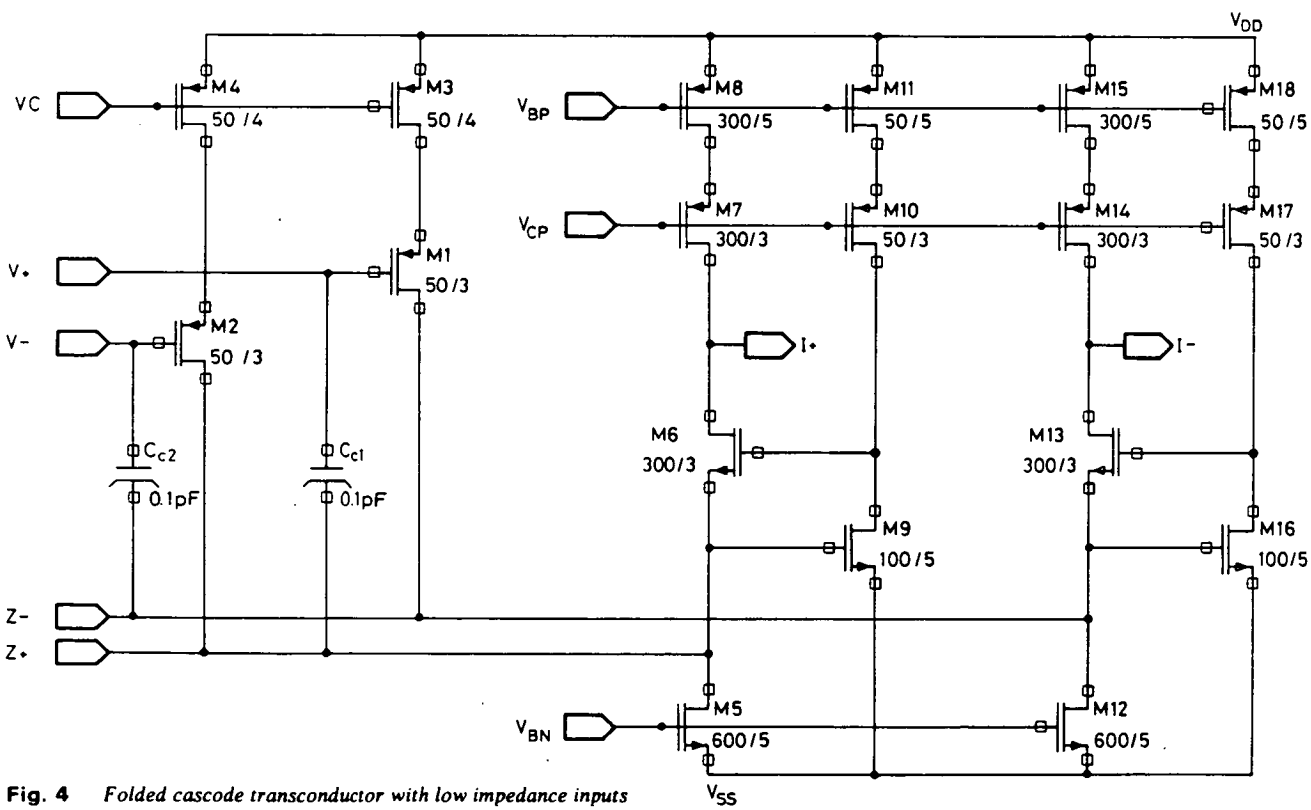

Fig. 4 *Folded cascode transconductor with low impedance inputs*

which adjusts the bias voltage V_{BN} so that the mean of the two output voltages remains close to midrail.

Care must be taken to ensure that the capacitors connected to the low impedance inputs do not cause the loops M6–M9 and M13–M16 to become unstable. If an input capacitor C_i is driven by signal V_i, the following high pass relation can be found by small signal analysis for the voltage V_Z at the $Z+$ node:

$$V_Z/V_i = s^2/[s^2 + s\omega_0/Q + \omega_0^2] \quad (9)$$

where

$$\omega_0 = \sqrt{(gm_6\, gm_9/C_i\, C_9)} \quad (10)$$

and

$$Q = \sqrt{(gm_9\, C_i/gm_6\, C_9)} \quad (11)$$

where C_9 is the capacitive load seen by M9 (which will be dominated by the gate capacitance of M6) and gm_i is the transconductance of M_i. For $Z+$ to remain a low impedance, ω_0 must be a frequency much greater than the filter passband. This condition will be satisfied by sufficiently high values of gm_6 and gm_9. For the gain loops within the transconductor to remain stable, the value of Q must not be too high. Eqn. 11 shows that this requires gm_6 to be somewhat greater than gm_9. In the present design, the values of ω_0 and Q are approximately 300 Mrad/s and 1.2, respectively.

The new transconductor was simulated using SPICE with level 3 models for a 1 μm p-well process. The results of the AC analysis are shown in Figs. 6 and 7. A 79.58 pF

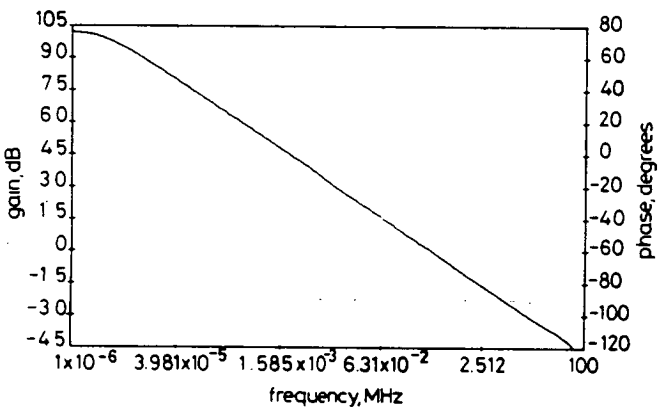

Fig. 6 *Simulated gain (solid line) and phase (dotted line) of transconductor-C building-block with respect to integrating input*

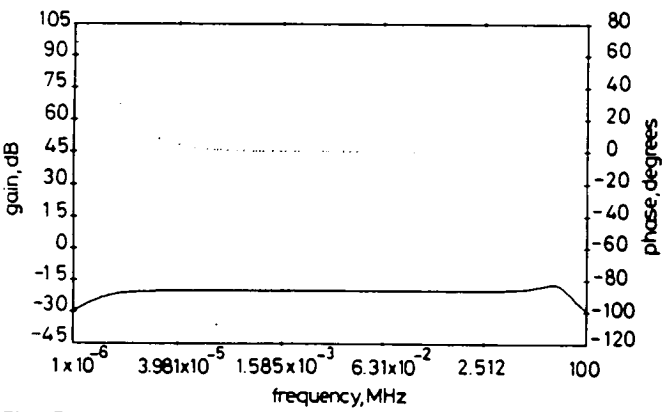

Fig. 7 *Simulated gain (solid line) and phase (dotted line) of transconductor-C building-block with respect to non-integrating input*

load was connected between each of the outputs and ground, giving an effective differential load of 39.79 pF and a unity gain frequency of 400 kHz for the nominal transconductance of 100 μS. Fig. 6 shows the gain and phase with respect to the integrating (high impedance) input. The phase at the unity gain frequency is $-90.01°$ which is close enough to the ideal value ($-90°$) to give very little distortion in a filter passband. This good phase performance is achieved by inclusion of the compensation capacitors C_{c1} and C_{c2} (both of value C_c). These introduce a high frequency zero (at circular frequency $2gm/C_c$) into the transfer function of the transconductor to provide first order cancellation of the effects of parasitic poles The optimum value of C_c is found by iteration of the AC simulation.

Fig. 7 shows the corresponding curves for the nonintegrating (low impedance) input with input capacitors of value 7.958 pF. In the region of 400 kHz the gain is within 0.1 dB of the correct value (-20 dB) and the phase shift is only 0.07°. The gain error is probably caused by the output capacitance of the transconductor.

Fig. 8 shows the output current as a function of input voltage. Fig. 9 represents the output error expressed as a

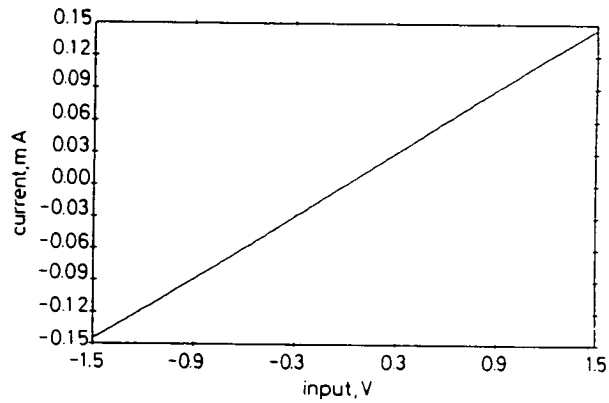

Fig. 8 *Simulated output current against input voltage for folded cascode transconductor with low impedance inputs*

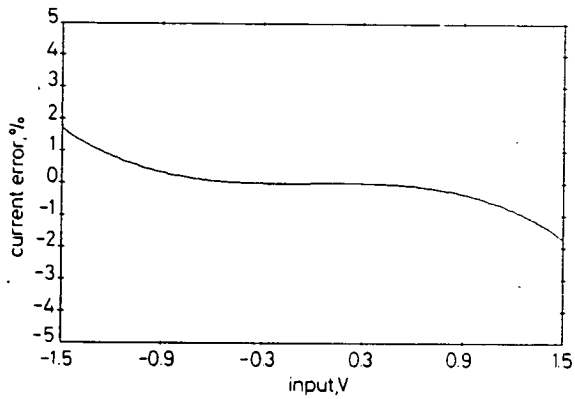

Fig. 9 *Error in output current as percentage of full scale*

percentage of the full scale current. For input voltages in the range ± 1 V, the output current is within 0.46% of the ideal value (100 μA at 1 V). The full scale current is equal to the quiescent current (300 μA) in the cascode devices, therefore the output current modulation in this range is 29.54%. The accuracy of this FC transconductor falls off gently with increasing input voltage, in contrast to the abrupt cutoff effect seen in single stage transconductors.

5 Bandpass filter design

The transconductor described has been used to design a sixth-order Chebyshev bandpass filter with 400 kHz centre frequency, 40 kHz bandwidth and 0.1 dB passband ripple. The passive prototype ladder is shown in Fig. 10, in which the following values were obtained for the

normalised response:

$$R_1 = R_2 = 1$$
$$C_3 = 8.4953 \quad (12)$$
$$C_1 = C_5 = 9.419$$
$$L_1 = L_3 = L_5 = 0.09685$$

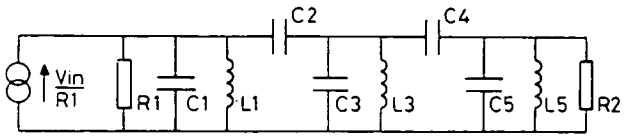

Fig. 10 *Passive prototype for sixth order Chebychev bandpass filter*

The resulting fully differential active circuit is shown in Fig. 11, the routing of control and bias voltages being omitted for clarity. Using conventional transconductors would have required a transconductance ratio of 10:1 to simulate the termination resistors. The same function is performed by capacitors CT_1 and CT_2 connected to the pensate actively for tolerances in the transconductor and capacitor values such that the filter transfer function remains correctly scaled with respect to the frequency of a reference clock signal. These tolerances arise from variations in process parameters and temperature, as well

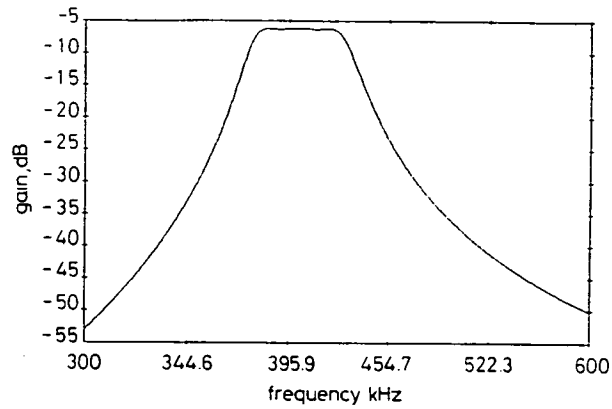

Fig. 12 *Simulated response of transconductor-C filter*

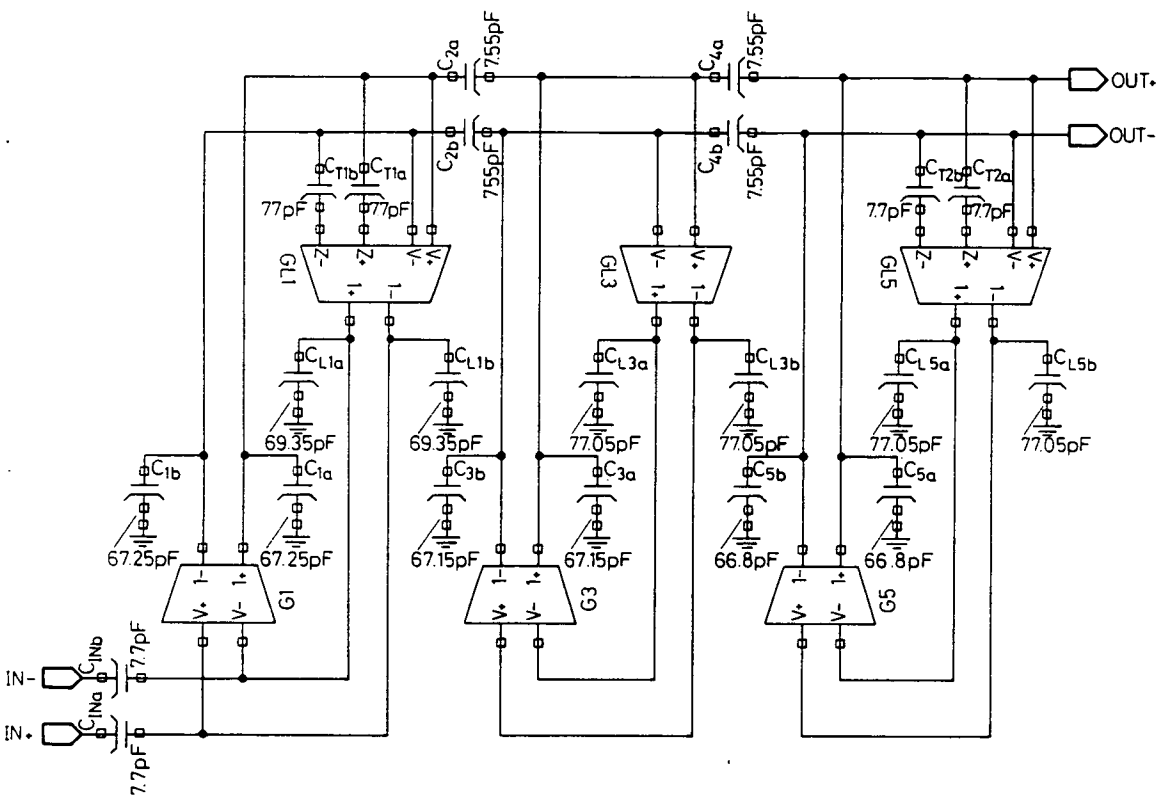

Fig. 11 *Fully differential transconductor-C bandpass ladder filter*

appropriate low impedance inputs. The transconductor and capacitor methods of termination are referred to as F-type and E-type, respectively, by analogy with corresponding methods in the design of switched capacitor biquad stages [8].

This filter, along with a frequency control loop, has been designed and layed out for a 1 μm p-well process and is currently in fabrication. The filter circuit was simulated at transistor level, with bottom plate parasitic capacitances included in the model and triode mode transistors broken into unit elements for optimum modelling of transmission line effects. The simulated AC response is shown in Fig. 12. The gain and ripple errors are approximately 0.1 dB and 0.01 dB, respectively.

The control loop is a phase locked loop, including a voltage controlled oscillator formed from the same transconductor used in the filter [1]. Its function is to compensate for inaccuracies in process characterisation. The control-loop generates the DC control voltage which sets the value of the transconductors in the filter. The control loop will not adversely affect the performance of the transconductors as long as the control voltage is adequately decoupled and remains reasonably close to its nominal value.

6 Conclusions

The problems of designing CMOS transconductors for high frequency bandpass ladder filters have been discussed and an original circuit overcoming these problems has been presented. The new circuit features a novel grounded-quad input stage, a very high output impedance and the facility of low impedance inputs to avoid the requirement for transconductance ratios in scaled

filters. The application of the new transconductor has been illustrated by the design of a high frequency sixth-order Chebyshev bandpass filter. The performance of the transconductor and the filter have been demonstrated by analysis and simulation results.

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MATRIX METHODS FOR THE DESIGN OF TRANSCONDUCTOR LADDER FILTERS

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Abstract
Matrix based methods for the design of transconductor ladder filters are presented. When transconductors with low impedance inputs are used these allow the realisation of highly selective bandpass responses using a single value of transconductance. If conventional transconductors are used, transconductor ratios can be restricted to the input and damping branches for any response. The new methods are illustrated by the design of a sixth order elliptic bandpass ladder.

I Introduction

In recent years much research has been directed towards the development of continuous time transconductor filters as an alternative to switched capacitor (SC) filters, particularly in the frequency range 100kHz to 10MHz. Whilst many linear transconductor circuits have been presented in the literature [1,2,3,4], significant problems have impeded the design of active filter structures in which they might be applied.

The problem addressed in this paper is how to design ladder filters without recourse to ratioed transconductances. Ratioed transconductors are undesirable because the transistors which determine the value of a particular transconductor can vary in size within only a small range without suffering from poor matching in one extreme or producing significant parasitic capacitance and high power consumption in the other. Moreover it is inconvenient for a designer to have to produce a different set of ratioed transconductors for each new filter design. This problem is unique to transconductor filters since the corresponding variables in RC and SC filters (resistors and sampling capacitors respectively) can be scaled relatively freely.

Most methods used to derive active RC and SC filters from passive prototypes have been based, explicitly or otherwise, on the simulation of nodal voltages and inductor currents. Examples of such filters are leapfrog and coupled biquad ladders, as well as circuits obtained by simulating inductors using gyrators. These methods have been applied successfully to the design of lowpass transconductor ladders [1,3] but they cannot generally be applied to bandpass ladders without the use of ratioed transconductor inputs [2,4,5]. This is due to the fact that when the voltages of a coupled biquad bandpass filter are scaled for dynamic range the summing coefficients between biquads take values which are lower than the coefficients within each biquad by a factor typically close to the fractional bandwidth of the filter. The problem is compounded for prototypes containing inductor loops or unequal termination resistors since these imply non-integer ratios that cannot be implemented by combinations of a unit transconductance.

In this paper we present matrix methods for the derivation of original transconductor bandpass ladders. A passive ladder can be represented by the matrix equation

$$J = (G+sC+s^{-1}\Gamma)V \qquad (1)$$

where V and J are vectors representing the nodal voltages and input current source and G, C, and Γ are matrices representing the contributions of conductors, capacitors and inductors respectively. This equation is decomposed into two first order equations by the introduction of a vector of intermediate variables. To form the active filter, each first order equation is implemented by a set of transconductor-C building blocks.

A set of transconductor filters has been designed by the methods described here and is currently in fabrication on a 1μ CMOS process. These filters have centre/cutoff frequencies in the range 400kHz-4MHz. Even higher frequencies could be reached by the use of bipolar or GaAs technologies [6].

II Transconductor-C Building Blocks

The general first order transconductor-C building block has the transfer function:

$$V_{out} = [\sum_i g_i V_i + s\sum_j C_j V_j]/sC \qquad (2)$$

It is desirable that only one value of g_i be used in a particular filter, but where more than one value is used the values should be in low integer ratios. Using a conventional transconductor, (2) is implemented by the circuit shown in Figure 1. In this case the capacitors C_j can represent only bidirectional coupling paths when driven by internal nodes, which can be a serious restriction. To obtain unidirectional coupling paths, a transconductor with low impedance current summing inputs [4] may be used, as shown in Figure 2. The low impedance input is marked Z and the integrating inputs are marked g1+,g1-, etc.

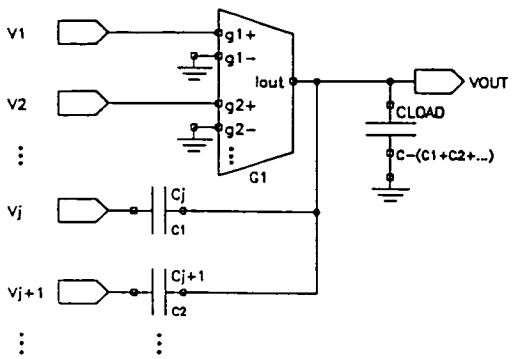

Figure 1 First order section using conventional transconductor

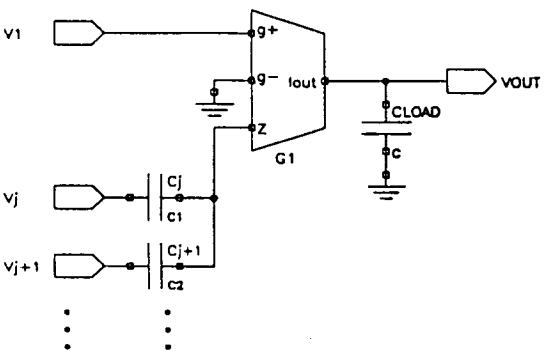

Figure 2 First order section using transconductor with low impedance inputs

III Matrix Decompositions

i. Topological Decomposition

The inductor admittance matrix is factorised as:

$$\Gamma = ADA^T \tag{3}$$

where D is a diagonal matrix whose elements are the reciprocals of the inductances in the prototype, and A is a conventional incidence matrix. The auxiliary variables are defined by:

$$X = (sg)^{-1}DA^TV \tag{4}$$

where g is a constant with the dimensions of conductance. Equations (3) and (4) are substituted into (1) to obtain

$$CV = s^{-1}[J-GV-gAX]. \tag{5}$$

The design equations (4) and (5) can be used to obtain conventional lowpass leapfrog filters. However new structures are required for the design of realisable bandpass filters. These are provided by the following two decompositions.

ii. Left Inverse Decomposition

The auxiliary variables are defined by

$$X = sCVg^{-1} \tag{6}$$

and (6) is substituted into (1), giving

$$gX = J-GV-s^{-1}\Gamma V. \tag{7}$$

The design equations are obtained by rearranging (6) and multiplying (7) by the inverse of Γ:

$$g^{-1}CV = s^{-1}X \tag{8}$$

$$g\Gamma^{-1}X = -s^{-1}V + \Gamma^{-1}[J-GV]. \tag{9}$$

iii. Right Inverse Decomposition

This proceeds as for Left Inverse Decomposition, except that X is defined:

$$gX = s^{-1}\Gamma V. \tag{10}$$

The resulting design equations are:

$$g\Gamma^{-1}X = s^{-1}V \tag{11}$$

$$g^{-1}CV = s^{-1}[g^{-1}(J-GV)-X]. \tag{12}$$

IV Bandpass Transconductor Ladders

If transconductors with low impedance inputs are available [4] the Left Inverse (LI) decomposition should be used. In (8) and (9) the only integrated terms are vectors so a single value of transconductance can be used throughout the whole filter. This value g is selected such that V and X are correctly scaled for dynamic range. We set $g = 1/\alpha R$ where the scaling parameter α often takes an optimum value close to the fractional bandwidth of the filter. As an example a sixth order elliptic bandpass filter with 400kHz centre frequency, 40kHz bandwidth, 0.1dB passband ripple and 50dB stopband attenuation has been designed. The passive prototype for this response, shown in Figure 3, can be described by the matrices:

$$J = \begin{pmatrix} \frac{V_{in}}{R_1} \\ 0 \\ 0 \end{pmatrix}, \quad V = \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix}, \quad G = \begin{pmatrix} \frac{1}{R_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{1}{R_2} \end{pmatrix},$$

$$C = \begin{pmatrix} C_1+C_2 & -C_2 & 0 \\ -C_2 & C_2+C_3+C_4 & -C_4 \\ 0 & -C_4 & C_4+C_5 \end{pmatrix}.$$

$$\Gamma = \begin{pmatrix} \frac{1}{L_1}+\frac{1}{L_2} & \frac{-1}{L_2} & 0 \\ \frac{-1}{L_2} & \frac{1}{L_2}+\frac{1}{L_3}+\frac{1}{L_4} & \frac{-1}{L_4} \\ 0 & \frac{-1}{L_4} & \frac{1}{L_4}+\frac{1}{L_5} \end{pmatrix} \qquad (13a\text{-}e)$$

Substituting (13a-e) into (8) and (9) and implementing each row by a first order section (Figure 2) leads to the transconductor ladder shown in Figure 4. Using the transconductor described in [4] this circuit was simulated with SPICE models for a 1μ p-well CMOS process. The magnitude response is given in Figure 5.

If transconductors with low impedance inputs are not available, the Right Inverse (RI) Decomposition provides the best bandpass ladders. Conventional transconductors can be used to implement (11) and (12) because the only non-integrated terms are those arising from the off-diagonal elements of Γ^{-1} and C, which represent bidirectional coupling paths. Neither V nor X is premultiplied before integration, so no unrealisable summing coefficients are introduced. In order to scale the filter correctly for dynamic range a second (smaller) value of transconductance is usually required to realise the input branch and filter terminations. This use of a second transconductance value is acceptable because it can be chosen to be in integer ratio to the first and it is used only to represent the termination resistors which are the least sensitive components of the prototype. This compares favourably with a cascaded biquad ladder in which unrealisable transconductor ratios can occur throughout the filter.

LI and RI filters employ capacitive and resistive damping respectively, hence we can refer to them as "E-type" and "F-type" circuits by analogy with the terminations and terminology used for SC biquads [7].

V Conclusions

The inverse matrix methods allow the design of bandpass transconductor ladders which would not be realiseable using conventional coupled-biquad or inductor simulation methods. The Topological Decomposition represents a formal method for the design of lowpass transconductor ladders. These techniques have been used to design a set of high frequency CMOS transconductor ladder filters which are currently in fabrication. Experimental results will be published when available.

Acknowledgements

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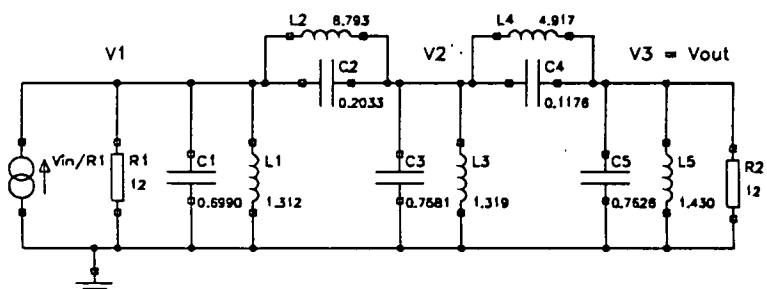

Figure 3 Sixth order elliptic bandpass prototype

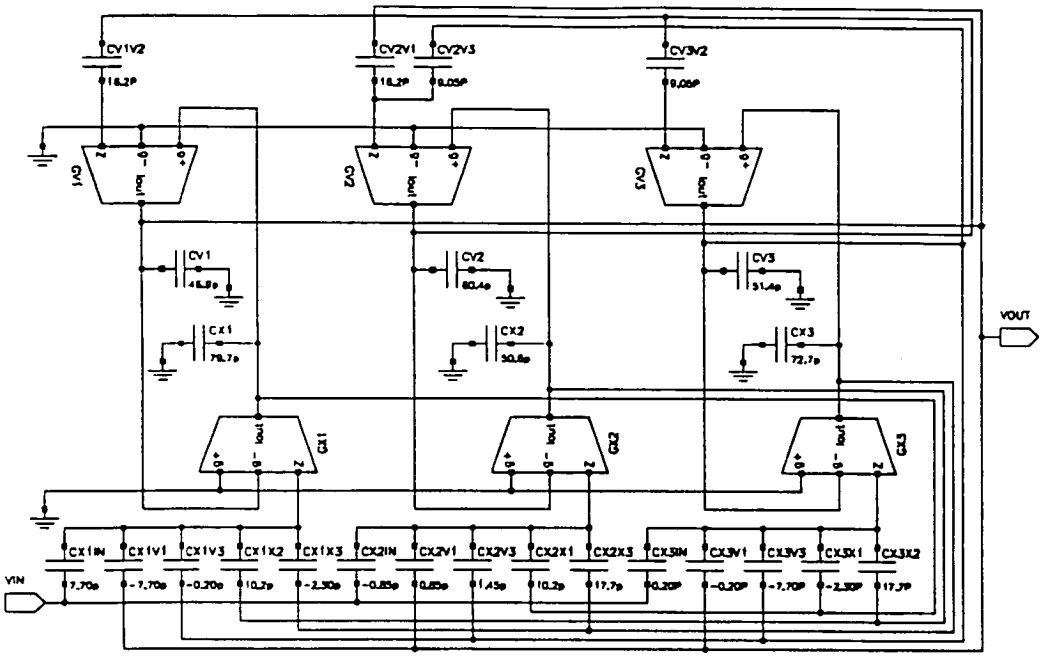

Figure 4 Left inverse transconductor ladder (single ended equivalent circuit)

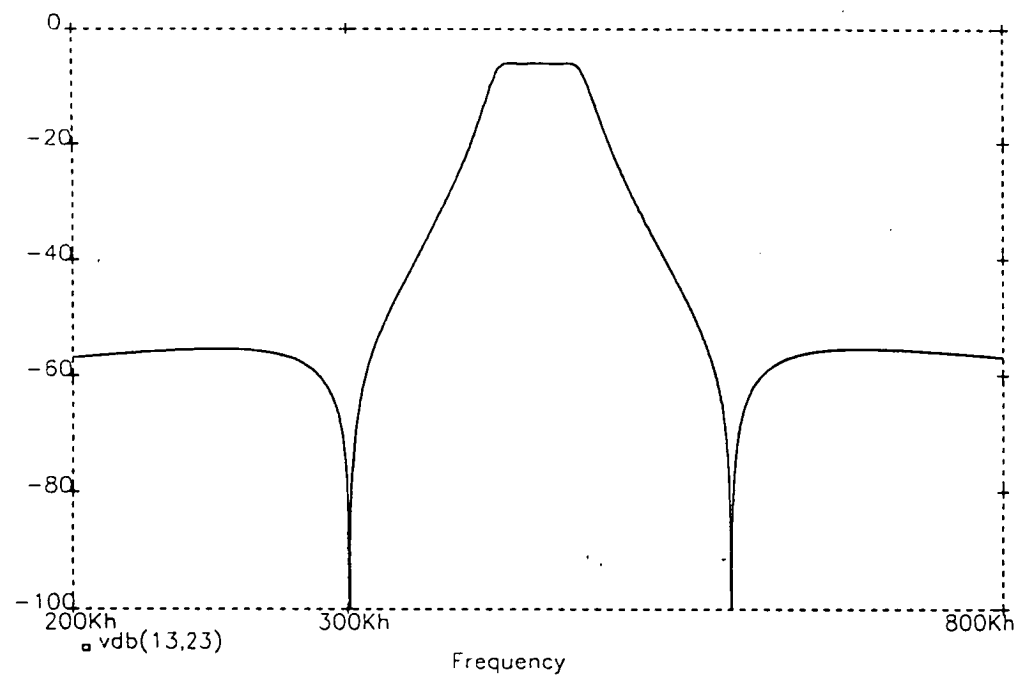

Figure 5 Simulated response of left inverse elliptic bandpass ladder

SOFTWARE FOR THE DESIGN OF TRANSCONDUCTOR-CAPACITOR FILTERS AND EQUALISERS

Lu Yue*, N.P.J.Greer**, and J.I.Sewell*

INTRODUCTION

Recently, realisation of continuous-time filters based on operational transconductance amplifiers and capacitors have received considerable attention. A number of design procedures for transconductor-capacitor filters have appeared in the literature[1-4], however comparatively little research has been carried out into transconductor filter and equaliser synthesis software. In this paper, a transconductor-capacitor filter synthesis software suite is described. Some notable features of the software are:

1. A user friendly interface is provided, based on the X-window system. The specifications of the filter can be read in from existing files or menus. Graphics edit facilities are offered to specify the templates of arbitrary and classical manitude filters, and group delay for equalisers.

2. Butterworth, Chebyshev, Inverse-Chebyshev and Elliptic approximation functions as well as arbitrary passband and stopband response approximations are available. In the arbitrary magnitude design mode, the desired amplitude response of the filter is specified by a pair of piece-wise linear boundaries (a template) of amplitude against frequency. The arbitrary response approximation program will attempt to fit a response within the upper and lower boundary[5].

3. A ladder based simulation approach is used to obtain transconductor-capacitor filter and equaliser circuits. Matrix decompositions are used to derive design methods - Topological Decomposition, Left Inverse Decomposition and Right Inverse Decomposition - for transconductor-capacitor filters and equalisers.

4. Optimisation for non-ideal factors is achieved by predistorting the attenuation specifications and re-designing the filter. This is a simple scheme but has the advantages of reducing the order of the problem and permitting easy control by the designer.

5. Group delay equalisation using ladder based all-pass networks[6] in transconductor-capacitor realisation is available.

LADDER BASED DESIGN METHODS

A passive ladder can be represented by the matrix equation

$$J=(G+sC+s^{-1}\Gamma)V \qquad (1)$$

where V and J are vectors representing the nodal voltages and input current source and G, C, and Γ are matrices representing the contributions of conductors, capacitors and inductors respectively. It is well known that a set of linear algebraic equations can represent a signal flow graph and be realized by an active-RC circuit. Equation (1) contains nonlinear combinations of the basic functions s^{-1}. To get a linear system, we can introduce a set of intermediate variables and decompose the system (1) into two inter-related systems. Each linear system is implemented by a set of transconductor-capacitor building blocks. It is desirable that only one value of transconductance be used, or if more than one value is required, the values should be in low integer ratios.

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i. Topological Decomposition

In topological decomposition, the auxilary variables are defined by:

$$X=(sg)^{-1}DA^{T}V \tag{2}$$

where D ia a diagonal matrix of the inverse inductance values of the prototype and A is a conventional incidence matrix of inductors and

$$\Gamma=ADA^{T} \tag{3}$$

From (1) and (2), we can get a design matrix for the topological decomposition as:

$$\begin{bmatrix} s^{-1}gA & C+s^{-1}G \\ g^{2}D^{-1} & s^{-1}gA^{T} \end{bmatrix}\begin{bmatrix} X \\ V \end{bmatrix}=\begin{bmatrix} s^{-1}J \\ 0 \end{bmatrix} \tag{4}$$

where g is a scaling factor with the dimension of transconductance. If the prototype ladder is equally terminated and g=1/R, the filter can be realized with one value transconductance. The auxiliary voltages X are directly proportional to the currents in the inductors of prototype ladder. The topological decomposition will generally lead to equivalent leapfrog topologies in active-RC, SC and transconductance-capacitor designs, if conventional transconductors are used. In the bandpass case, this decomposition can not be guaranteed to generate a stable active circuit and alternative decompositions are required.

ii. Right Inverse Decomposition

The auxiliary variables are defined by

$$X=(s^{-1}\Gamma V)/g \tag{5}$$

The resulting design matrix is:

$$\begin{bmatrix} g^{2}\Gamma^{-1} & -s^{-1}gI \\ s^{-1}gI & C+s^{-1}G \end{bmatrix}\begin{bmatrix} X \\ V \end{bmatrix}=\begin{bmatrix} 0 \\ s^{-1}J \end{bmatrix} \tag{6}$$

In (6), the integrated vector V is premultiplied by a matrix $s^{-1}G$. Only when the prototype ladder has equal resistance at both terminations and g=1/R, would the transconductor-capacitor filter require one transconductance value in the complete realisation. This decomposition will utilize the conventional transconductor building block shown in Fig.1(a). In the final design, stray capacitances have to be estimated and the circuit capacitances adjusted accordingly.

iii. Left Inverse Decomposition

This decomposition provides a solution to the equal value transconductance problem and eliminates the need for compensation of parasitic capacitances. The auxiliary variables in the Left Inverse Decomposition are defined by

$$X=(sCV)/g \tag{7}$$

and (7) is substituted into (1), giving

$$\begin{bmatrix} g^{2}\Gamma^{-1} & s^{-1}gI+g\Gamma^{-1}G \\ -s^{-1}gI & C \end{bmatrix}\begin{bmatrix} X \\ V \end{bmatrix}=\begin{bmatrix} g\Gamma^{-1}J \\ 0 \end{bmatrix} \tag{8}$$

The important feature of (8) is that both of the integrated vectors are premultiplied by a diagonal matrix with same elements. This allows the equations to be implemented as a transconductor-capacitor circuit with a single value of transconductance.

There are a number of other variations on the Left Inverse Decomposition with different costs in practical terms, regarding number of capacitors and the spread in capacitance.

To facilitate the realisation of these decompositions, the new low impedance input transconductors shown in Fig.1(b) are required[4]. These have the added attraction of nullifying the effects of parasitic capacitance.

CIRCUIT REALISATION

In normal circuit realisation, fully differential versions are generally required for many practical reasons. This also allows any negative capacitance values to be accommodated. Figs 2 and 3 show the Left and Right Inverse Decompositions for a 6th order bandpass realisation (single ended versions). The contrasting topologies are evident.

GROUP DELAY EQUALISERS

The features of ladder based allpass group delay equalisers networks[6] can be retained for transconductor-capacitor realisations. The three basic decompositions have been used in an extended mode to produce transconductor-capacitor equalisers, which are particularly attractive for higher frequency operation.

PROGRAM IMPLEMENTATION

The general procedure for filter and equaliser design is:

Step 1: Filter amplitude approximation
Step 2: Prototype ladder design
Step 3: Filter realisation
Step 4: Group delay approximation
Step 5: Prototype equaliser design
Step 6: Equaliser realisation

The software structure allows the user to employ an arbitrary filter approximation, when he can investigate the use of high order touch points[5] to reduce group delay equalisation requirements and hence minimize the circuit order of the equaliser employed.

The procedure for transconductor-capacitor circuit realisation is

Step 1: get G, Γ, and C matrix from prototype ladder filter
Step 2: set up matrix equation (4), (6), or (8)
Step 3: determine each submatrix type
Step 4: calculate all capacitor values
Step 5: construct transconductor-capacitor circuit
Step 6: post-processing of circuit
Step 7: output circuit netlist in SPICE format

The network realised by the proposed scheme will sometimes be inefficient in terms of hardware, since there may be two or more capacitors connected between same nodes. In step 6, a post-processing of the circuit procedure can remove redundant components.

The cost of the design process is very small. Once the components matrices G, Γ, and C have been set up by a summation of stamps, only one matrix inversion and usually less then three matrix multiplications need be applied. The matrix order is equal to the order of prototype ladder filter. A program for transconductor-capacitor ladder filter and equaliser design.

using both conventional and low impedance input transconductors is included in the XFILT suite.

A simple optimisation technique is avaliable for the correction of non-ideal factors in the transconductors such as bandwidth and transconductance value variations. Applications to filter topologies will be shown.

DESIGN EXAMPLES

A typical video filter and group delay equaliser was designed using the software. Fig.4 gives a 5th order lowpass filter amplitude response. In the passband, the group delay variation is 1.1us. When a 6th order group delay equaliser is used, the group delay variation is reduced to 0.2us. If a 12th order group delay equaliser is used, the group delay variation is reduced to 0.13us. Fig.5(a) gives the 6th order group delay equaliser response and Fig.5(b) gives the 12th order group delay equaliser response. Although the 12th order group delay equaliser has very good response, the 6th order group delay equaliser already satisfies specifications. The 5th order amplitude filter and 6th order group delay equaliser have been incorporated in a layout for fabrication. When a general IIR filter approximation is used, manipulation of touch points reduces the group delay equalisation requirements significantly. This permits a 5th order filter and a 4th order equaliser to satisfy the design specifications.

The second example is a 6th order bandpass filter and 10th order equaliser design. Both Left Inverse Decomposition and Right Inverse Decomposition can be used in the amplitude filter design. Fig.6 a) gives amplitude response and Fig.6b) gives group delay response. Before equalisation, the in-band group delay variation is 1.1ms and after equalisation, the group delay variation is 0.15ms.

CONCLUSIONS

Powerful software for the design of transconductor-capacitor filters and equalisers is presented. A user friendly interface is provided. Arbitrary, as well as Butterworth, Chebyshev, Inverse-Chebyshev and Elliptic approximations are available. Ladder based simulation approach and matrix decomposition methods are used to obtain transconductor-capacitor filter and equaliser circuits. The software is also capable of designing active-RC and SC circuits. Several designs have been obtained by using the software. The video amplitude filter and group delay equaliser are in fabrication.

ACKNOWLEDGEMENTS

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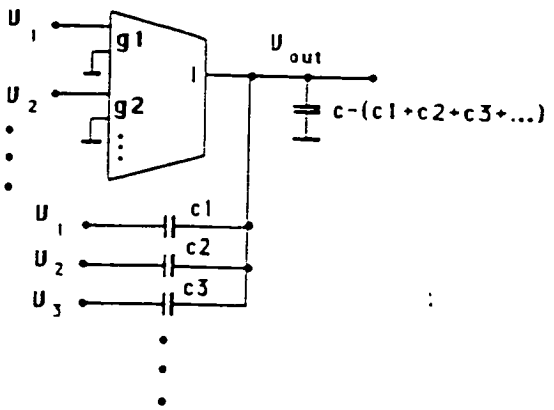

Fig.1(a) First Order Section Using Conventional Transconductor

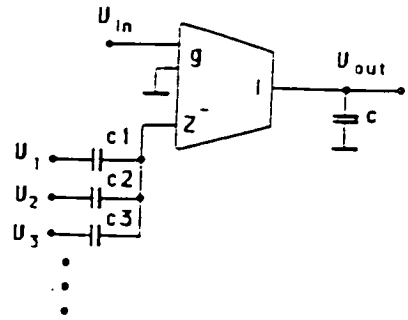

Fig.1(b) First Order Section Using Transconductor With Low Impedance Inputs

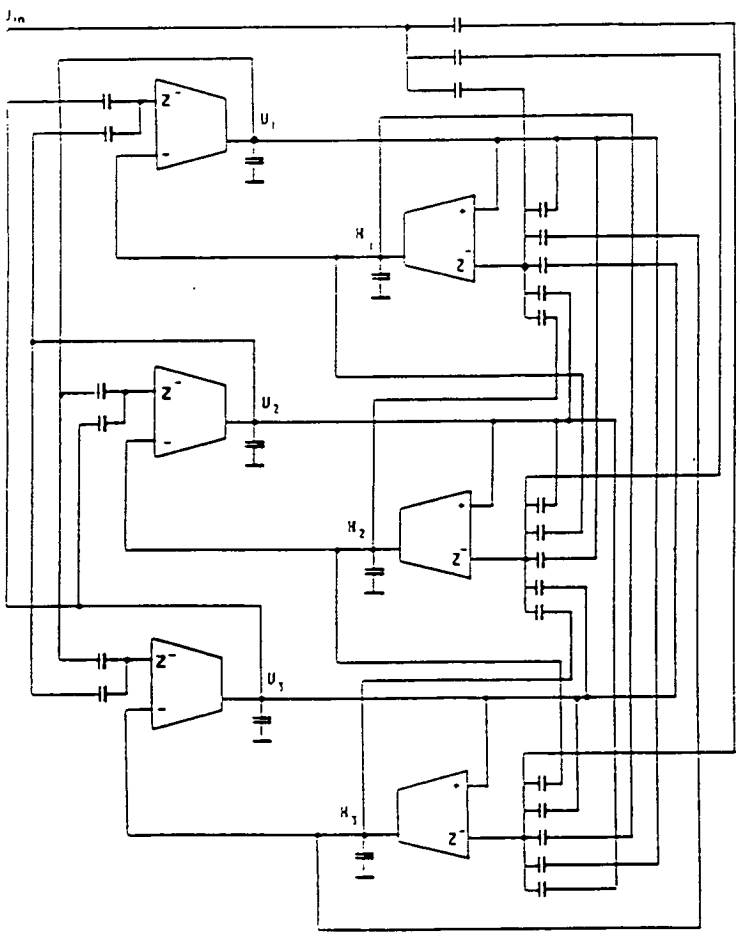

Fig.2 Left Inverse Transconductor-Capacitor Circuit Realisation

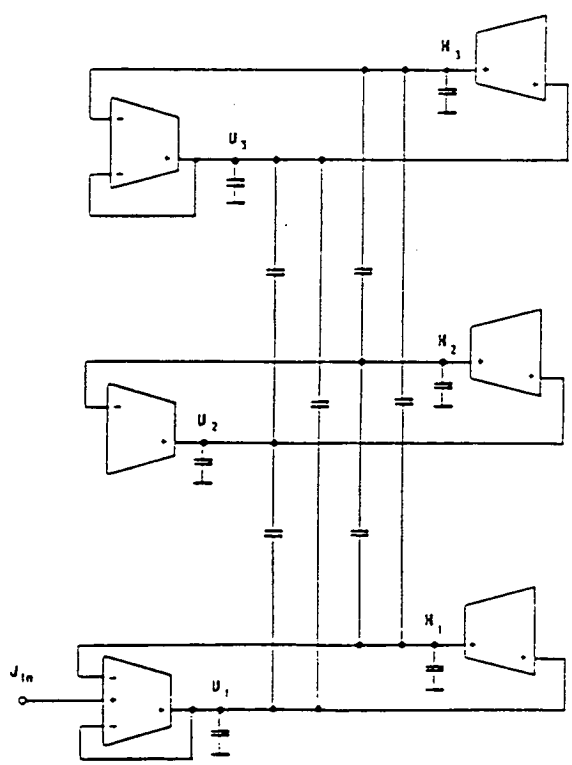

Fig.3 Right Inverse Transconductor-Capacitor Circuit Realisation

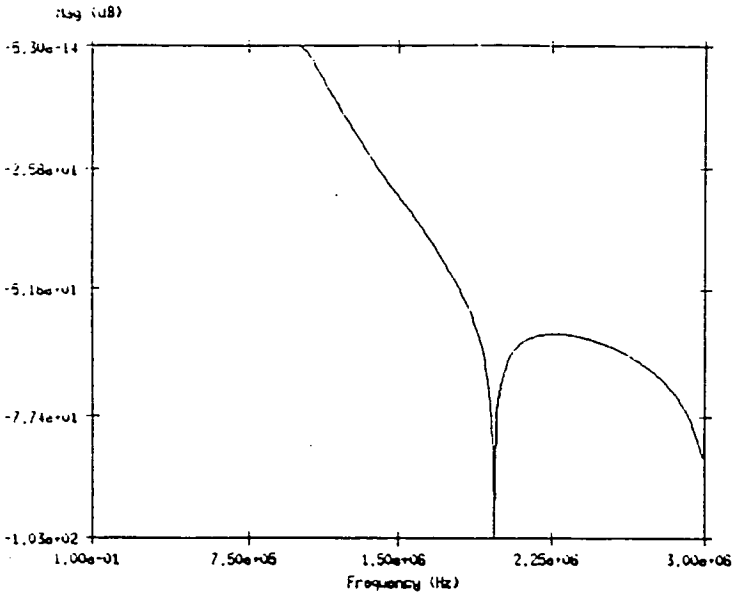

Fig.4 5th Order Video Filter Amplitude Response

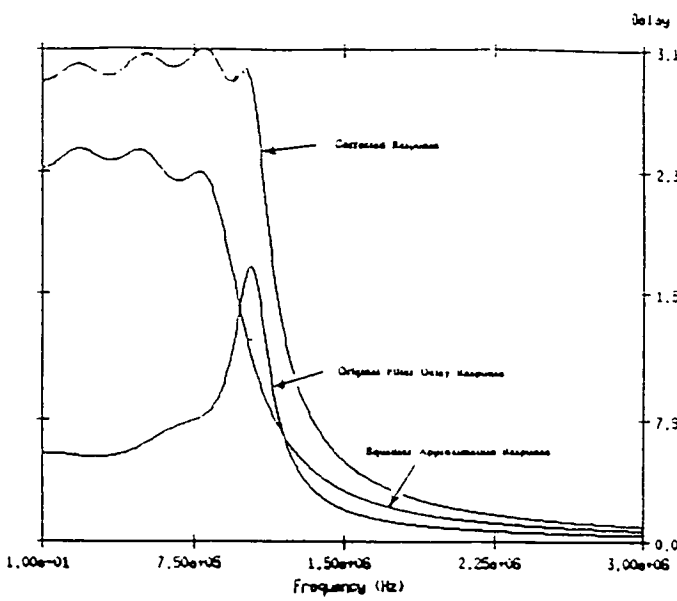

Fig.5(a) 6th Order Video Equaliser Group Delay

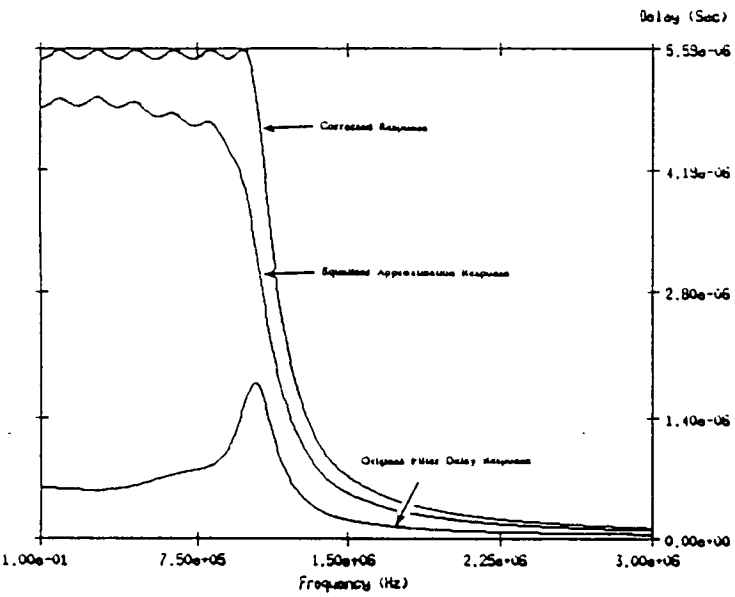

Fig.5(b) 12th Order Video Equaliser Group Delay

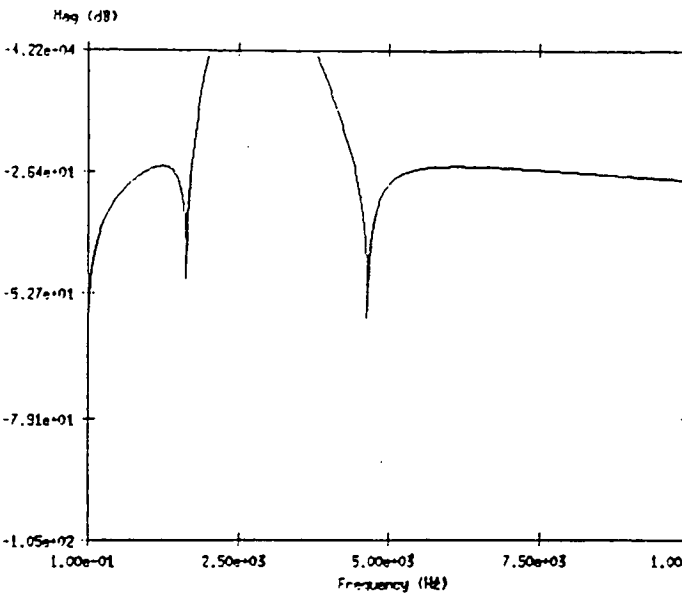

Fig.6(a) 6th Order Bandpass Filter Amplitude

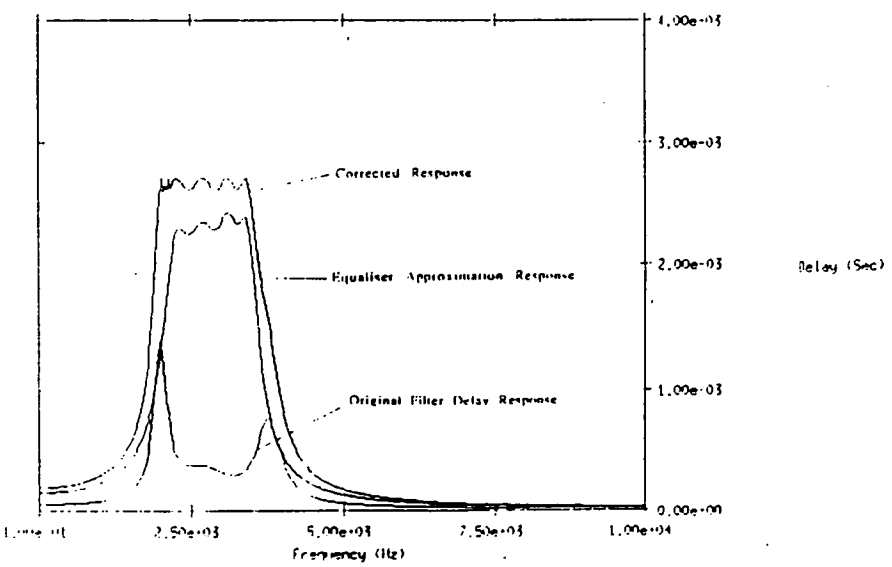

Fig.6(b) Equalisation Response With 10th Order Equaliser